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# Hole trapping capability of silicon carbonitride charge trap layers★

Kiyoteru Kobayashi* and Hiroshi Mino

Graduate School of Engineering, Tokai University, 4-1-1 Kitakaname, Hiratsuka, Kanagawa 259-1292, Japan

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**Abstract.** We have evaluated the hole trapping capability of the silicon carbonitride (SiCN) dielectric film for application in metal-oxide-nitride-oxide-silicon (MONOS)-type non-volatile memory devices. After a great number of holes were injected to the SiCN charge trap layer of memory capacitors at high applied voltages, the flat-band voltage shift $\Delta V_{fb,h}$ of the capacitors was saturated and the charge centroid location of holes trapped in the SiCN layer was found to reach at 1.8–2.0 nm from the blocking oxide-charge trap layer interface. Using the obtained $\Delta V_{fb,h}$ and charge centroid values, the maximum density of holes trapped in the SiCN layer was estimated to be $1.2 \times 10^{13}$ holes/cm$^2$, which was higher than that trapped in a silicon nitride charge trap layer ($=1.0 \times 10^{13}$ holes/cm$^2$). It is concluded that the high density of trapped holes caused large $\Delta V_{fb,h}$ in the memory capacitors with the SiCN layer.

## 1 Introduction

The metal-oxide-nitride-oxide-semiconductor (MONOS) architecture is becoming more important as an attractive solution for low-power-consumption embedded non-volatile memories (NVMs) [1–11] and three-dimensional (3D) NAND flash memories [12–15]. In this architecture, charge carriers are injected from the silicon body to the charge trap layer and are captured by trap sites existing in the layer. The trapped carriers cause a shift in the threshold voltage of MONOS-type memory transistors, which is applied to data storage. Over the last several decades, silicon nitride films have been employed as the charge trap layer since point defects in the films create energetically deep trap states for electrons and holes. Recently, to increase the bit density of NAND flash memories, enhanced multi-level cell technologies have been introduced, which have demanded a larger threshold voltage shift [15,16]. Since the value of threshold voltage shift is a function of the density of trapped carriers, exploring new charge trap materials that can trap a high density of carriers is one of crucial issues in order to implement high-bit-density NAND flash memories.

Previous studies using electron spin resonance have shown that silicon dangling bonds are present in high density in a silicon carbonitride (SiCN) dielectric film grown by a plasma-enhanced chemical vapor deposition (PECVD) technique [17–19]. Therefore, charge trap states were expected to exist in high density in the film. Then, in several studies, SiCN-based charge trap memory devices were experimentally produced and a high erasing speed was achieved in one of the trial products [20]. It was also revealed that energetically deep trap states are present in high density in the SiCN dielectric film. The trap states for electrons were found to be distributed from 0.8 to 1.3 eV below the conduction band edge in SiCN bandgap [21]. The energy depth of trap states is comparable with that in silicon nitride films. Thus, the SiCN dielectric film has been suggested to be a potential candidate for the charge trap layer. However, the capability of trapping carriers, tolerance for write and read disturb and so on of the SiCN film still remain unclear.

The density of carriers trapped in the charge trap layer can be estimated using the charge centroid of trapped carriers and the value of flat-band voltage shift which is extracted from the capacitance–voltage (C–V) characteristics measured before and after carrier injection into the layer. Therefore, to determine the charge centroid of trapped carriers, the constant-voltage carrier injection method [22–25] and the constant-current carrier injection (CCCI) method [26] have been presented in several studies. However, both of the methods developed in those studies can be used only when the leakage current flowing through the charge trap layer during the carrier injection is negligible. To evaluate the carrier trapping capability of a new charge trap material, it is necessary that a great number of carriers are injected to the charge trap layer consisting of the material in the presence of a large electric potential difference between the gate electrode and the silicon body. In such a condition, since the leakage current flowing through the charge trap layer is not negligible, neither method can be used to extract the charge centroid of trapped carriers. As a solution to this issue, Mino and Kobayashi have recently proposed a method based on the analysis of Fowler-Nordheim (F–N) tunneling current through the blocking oxide film [27], which is termed as F–N current (FNC) method.

In the present work, we determine the charge centroid of holes trapped in the SiCN charge trap layer using the FNC method. The maximum density of holes trapped in

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* e-mail: kkbys@keyaki.cc.u-tokai.ac.jp

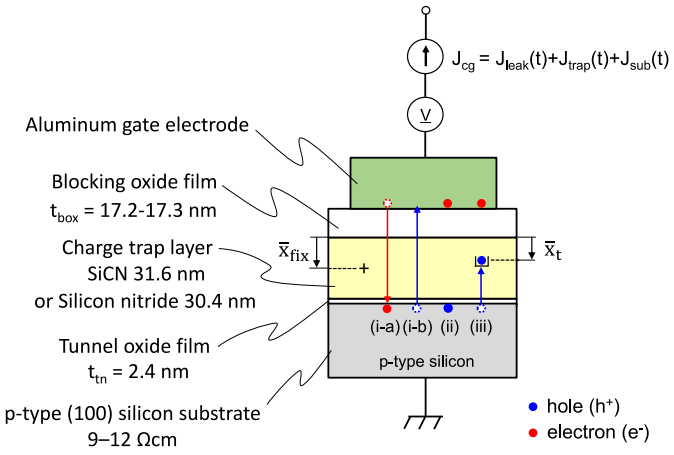


**Fig. 1.** Measurement configuration for obtaining the charge centroid $\overline{x}_t$ of holes trapped in the SiCN charge trap layer. $\overline{x}_t$ is measured from the interface between the blocking oxide film and the charge trap layer. $\overline{x}_{fix}$ is the charge centroid of fixed positive charge, which is also measured from the interface. The arrows (i-a) and (i-b) indicate the electron and hole flows through the stacked films, respectively. Item (ii) indicates hole accumulation at the silicon surface and the arrow (iii) indicates hole capture by empty trap sites.

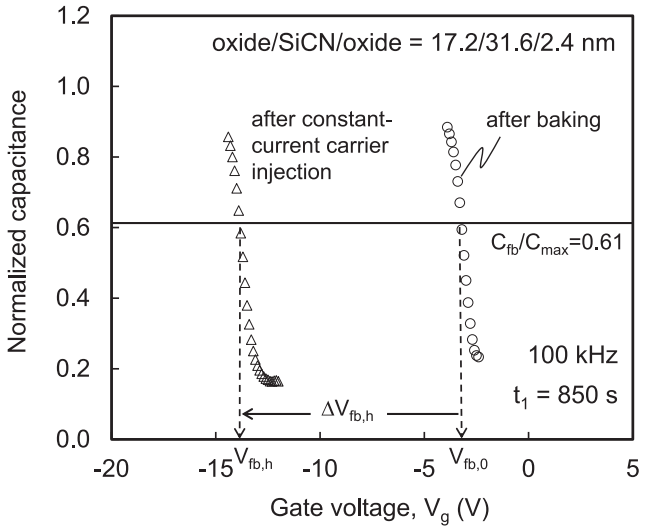


**Fig. 2.** C–V characteristics of the memory capacitor with the OCO stacked films after baking at 235 °C and after the constant-current carrier injection for 850 s. The flat-band voltage of the baked capacitor was determined to be −3.4 V by analyzing the C–V characteristics, which is termed as $V_{fb,0}$. The flat-band voltage shift $\Delta V_{fb,h}$ induced by holes trapped in the SiCN charge trap layer was obtained from $V_{fb,0}$ and $V_{fb,h}$.

the SiCN layer is estimated using the determined charge centroid location. We also make a comparative study of the hole trapping capabilities of SiCN and silicon nitride charge trap layers.

## 2 Sample preparation

Memory capacitors with blocking oxide-SiCN-tunnel oxide (OCO) stacked films were used in this work. Figure 1 shows a cross sectional view showing the memory capacitors. A 2.4-nm-thick tunnel oxide film was grown by rapid thermal oxidation of p-type (100) silicon substrates. An SiCN film of 31.6 nm in thickness was formed from a gas mixture of $Si(CH_3)_4$ and $NH_3$ at 400 °C by a PECVD technique. A blocking oxide film of 17.2–17.3 nm in thickness was formed at 400 °C by PECVD. Finally, aluminum gate electrodes were formed on the fabricated stacked dielectric films using a vacuum evaporation apparatus and a stencil mask. The high-frequency C–V characteristics were measured to determine the flat-band voltage of the memory capacitors using an Agilent E4980A LCR meter.

The optical properties of the SiCN film were measured by means of the spectroscopic ellipsometry. The refractive index was found to be 1.91 at a wavelength of 632.8 nm. The band gap was estimated to be 3.4 eV using the Tauc method. The relative dielectric constant was obtained to be 4.8 from a combination of the capacitance measurement and spectroscopic ellipsometry. X-ray photoelectron spectroscopy (XPS) measurements were performed to determine the band-offset value between the top of the valence band of the SiCN film and that of the silicon substrate using an ULVAC-PHI Quantera SXM spectrometer with a monochromatic Al Kα (1486.6 eV) X-ray source, which was found to be 1.7 eV. The atomic ratios of carbon to silicon and of nitrogen to silicon in the SiCN film were also obtained to be $0.77 \pm 0.06$ and $0.41 \pm 0.04$, respectively, by XPS measurements, which were nearly constant throughout the film thickness.

In Section 3, we compare the hole trapping capability of the OCO stacked films with that of blocking oxide-silicon nitride-tunnel oxide (ONO) stacked films which was reported in reference [27]. The ONO stacked films have also the same structure as the OCO stacked films, as shown in Figure 1. The silicon nitride film of 30.4 nm in thickness was grown from a gas mixture of $Si_2Cl_6$ and $NH_3$ at 600 °C in a low-pressure chemical vapor deposition reactor. The refractive index at a wavelength of 632.8 nm and the relative dielectric constant of the silicon nitride film were determined to be 1.97 and 7.3, respectively.

In this study, to evaluate the hole trapping capability, we need to investigate the hole trapping phenomenon by empty trap sites in the SiCN charge trap layer. Therefore, all the fabricated memory capacitors were baked at 235 °C for longer than two weeks to emit electrons and holes trapped in the layer.

## 3 Results and discussion

Figure 2 shows the C–V characteristics of the memory capacitor with the OCO stacked films. The flat-band voltage of the capacitor baked at 235 °C was determined to be −3.4 V by analyzing the C–V characteristics, which is termed as $V_{fb,0}$. This negative value in $V_{fb,0}$ denotes that a fixed positive charge existed in the stacked films after baking the memory capacitor.

Subsequently, a constant-current power source was connected to the gate electrode with grounding the silicon substrate. The gate current density $J_{cg}$ was maintained at a

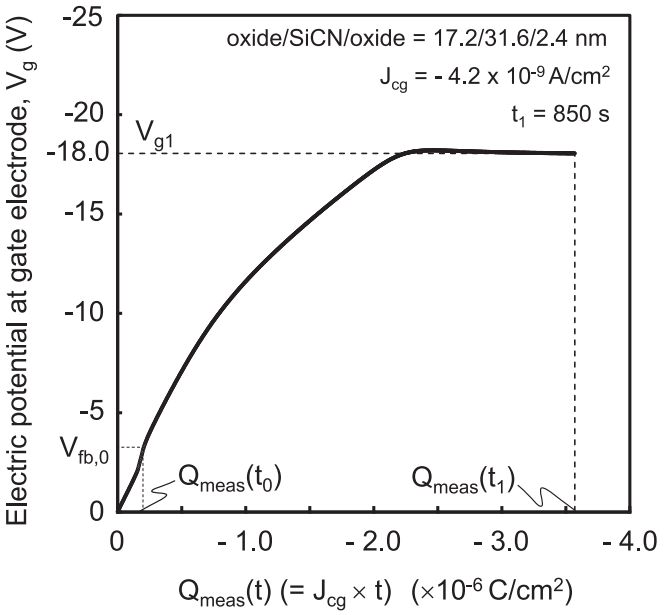


**Fig. 3.** Variation of electric potential at the gate electrode $V_g$ of the memory capacitor with the OCO stacked films during the constant-current carrier injection. The gate current density $J_{cg}$ was maintained at a constant value of $-4.2 \times 10^{-9}$ A/cm$^2$ for 850 s. $Q_{meas}(t)$ is defined by $Q_{meas}(t) = J_{cg} \times t$ with $J_{cg}$ and time t during which the gate current flows. As $Q_{meas}(t)$ increased, $V_g$ changed, and then converged at $-18.0$ V. $t_0$ is defined as the time at which $V_g$ reached $V_{fb,0}$. $t_1$ is defined as the time when the gate current flow was shut off and $V_{g1}$ is defined as the electric potential at the gate electrode at time $t_1$.

constant value of $-4.2 \times 10^{-9}$ A/cm$^2$ for a certain period of time and the negative electric potential at the gate electrode $V_g$ was measured. Figure 3 shows $V_g$ of the OCO memory capacitor versus $Q_{meas}(t)$. Here, $Q_{meas}(t)$ is defined by $Q_{meas}(t) = J_{cg} \times t$ with $J_{cg}$ and time t during which the gate current flows. As $Q_{meas}(t)$ increased, $V_g$ changed from 0 V and then converged at $-18.0$ V. The memory capacitor was under inversion or depletion condition when $V_g$ ranged from 0 to $V_{fb,0}$. In this figure, $t_0$ is defined as the time at which $V_g$ reached $V_{fb,0}$. $t_1$ is defined as the time when the gate current flow was shut off and $V_{g1}$ is defined as the electric potential at the gate electrode at time $t_1$. Figure 4a shows the energy band diagram of the OCO memory capacitor at time $t_0$ ($V_g = V_{fb,0}$). In Figure 4a, it is assumed that the fixed positive charge forms a sheet of charge and the centroid $\overline{x}_{fix}$ of the charge, measured from the SiCN-blocking oxide interface, was located at the middle of the charge trap layer [27]. After $V_g$ exceeded $V_{fb,0}$, holes were accumulated at the silicon surface. As shown in Figure 4b, some of the holes were injected to the SiCN layer through the ultra-thin tunnel oxide film owing to the quantum mechanical tunneling and were captured by empty trap sites in the SiCN layer. Figure 4c shows the energy band diagram of the OCO memory capacitor at $t = t_1 = 850$ s ($V_g = V_{g1} = -18.0$ V), which is drawn taking account of the electric fields caused by the electric potential at the gate electrode, trapped holes and the fixed positive charge. The values of

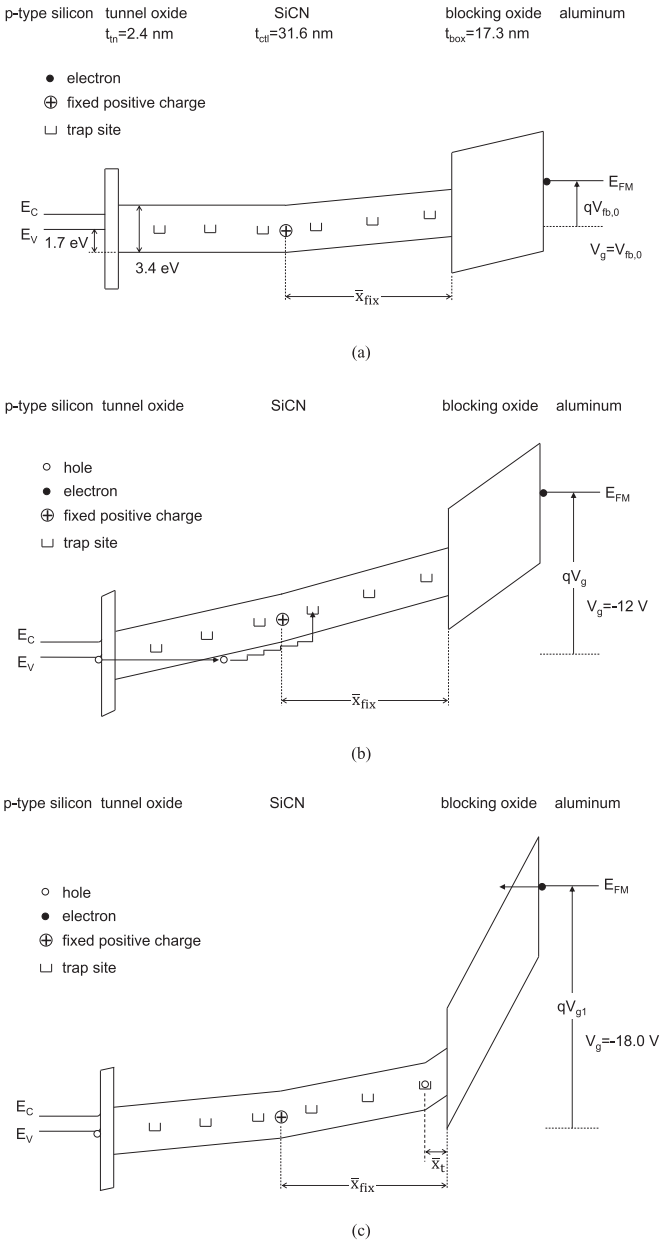


**Fig. 4.** Schematic energy band diagrams of the OCO memory capacitor for $t = t_0$ ($V_g = V_{fb,0}$) (a), for $t_0 < t < t_1$ ($V_{fb,0} < V_g < V_{g1}$) (b), and for $t = t_1 = 850$ s ($V_g = V_{g1} = -18.0$ V) (c).

the density and the charge centroid location of trapped holes used to calculate the electric fields will be shown later. After the hole injection, the C–V measurement was again conducted to determine the flat-band voltage $V_{fb,h}$. As shown in Figure 2, the C–V curve was shifted to the negative gate voltage direction due to hole trapping in the SiCN layer. The flat-band voltage shift $\Delta V_{fb,h}$ was estimated from $V_{fb,h}$ minus $V_{fb,0}$. $\Delta V_{fb,h}$ values were obtained for varying time periods $t_1$.

$J_{cg}$ consists of three current components and is written as $J_{cg} = J_{leak}(t) + J_{sub}(t) + J_{trap}(t)$. Here, $J_{leak}(t)$ is the leakage current component consisting of electron and hole flows through the OCO stacked films, $J_{sub}(t)$ is the

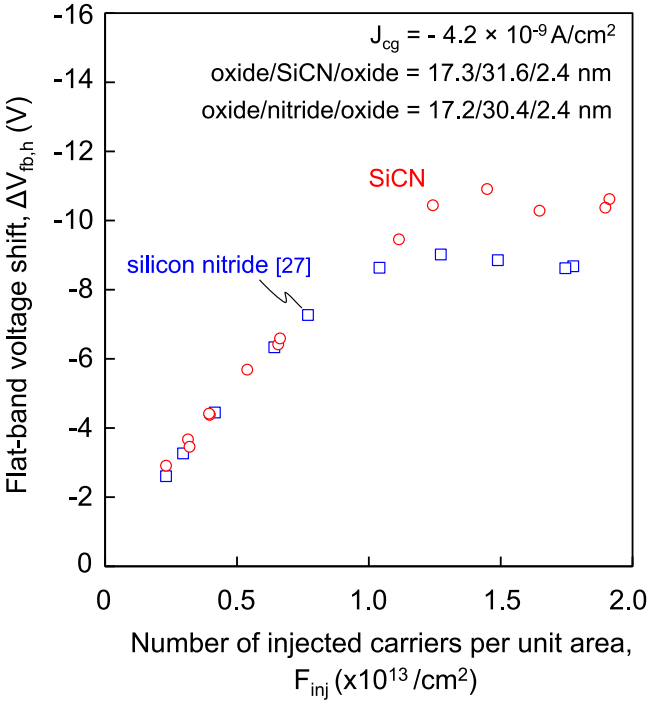


**Fig. 5.** Flat-band voltage shift $\Delta V_{\mathrm{fb,h}}$ of two kinds of memory capacitors with the OCO and ONO stacked films as a function of the number of injected carriers per unit area $F_{\mathrm{inj}}$.

displacement current component induced by hole accumulation at the silicon surface, and $J_{\mathrm{trap}}(t)$ is the displacement current component caused by hole trapping in the SiCN charge trap layer. Integrating $-J_{\mathrm{trap}}(t)$ over the interval $t_0$ to $t$ in time $(t_0 \leq t)$ gives the positive charge $Q_{\mathrm{trap}}(t_0,\ t)$ originated from trapped holes. Likewise, time integrals of $-J_{\mathrm{leak}}(t)$ and $-J_{\mathrm{sub}}(t)$ over the interval $t_0$ to $t$ yield $Q_{\mathrm{leak}}(t_0,\ t)$ and $Q_{\mathrm{sub}}(t_0,\ t)$, respectively. Here, $Q_{\mathrm{sub}}(t_0,\ t_1)$ is given by an integral of the capacitance of the memory capacitor after the carrier injection over the interval $V_{\mathrm{g1}}$ to $V_{\mathrm{fb,h}}$. Therefore, the number of injected carriers per unit area $F_{\mathrm{inj}}(t_1)$ can be experimentally determined by

$$F_{\mathrm{inj}} = \left\{-J_{\mathrm{cg}} \times (t_1 - t_0) - Q_{\mathrm{sub}}(t_0, t_1)\right\}/q, \qquad (1)$$

where $q$ is the elementary charge. The $\Delta V_{\mathrm{fb,h}}$ values obtained for various periods $t_1$ are shown in Figure 5 as a function of $F_{\mathrm{inj}}$. $\Delta V_{\mathrm{fb,h}}$ changed with increasing $F_{\mathrm{inj}}$, and was subsequently saturated. $\Delta V_{\mathrm{fb,h}}$ values of the ONO memory capacitors shown in reference [27] are also plotted in Figure 5. At large $F_{\mathrm{inj}}$'s, $\Delta V_{\mathrm{fb,h}}$ of the OCO structure was clearly larger than that of the ONO structure.

In Figure 3, $V_{\mathrm{g}}$ is a function of positive charge $Q_{\mathrm{trap}}(t_0,\ t)$ and $Q_{\mathrm{sub}}(t_0,\ t)$. The convergence of $V_{\mathrm{g}}$ indicates that $Q_{\mathrm{trap}}(t_0,\ t)$ and $Q_{\mathrm{sub}}(t_0,\ t)$ became constant. Therefore, we claim that $J_{\mathrm{trap}}(t)$ and $J_{\mathrm{sub}}(t)$ are negligible and $J_{\mathrm{leak}}(t)$ is dominant in $J_{\mathrm{cg}}$ when $V_{\mathrm{g}}$ reached $-18.0$ V. $J_{\mathrm{leak}}(t)$ consists of two current components: (a) the current component owing to F–N electron tunneling from the gate electrode and (b) the current component owing to hole injection from the silicon substrate. In the present study, the thickness of the blocking oxide film was designed to be sufficiently thick for electrons to follow the F–N tunneling mechanism. The probability of the F–N electron tunneling is abruptly increased as the electric field in the blocking oxide film is increased. Therefore, as can be seen in Figure 4c, the high oxide field caused by the negative electric potential at the gate electrode, $Q_{\mathrm{trap}}(t_0,\ t_1)$ and the fixed positive charge yields a high tunneling probability of electrons. Therefore, the current component owing to F–N electron tunneling would be dominant in $J_{\mathrm{leak}}(t)$, which is the dominant part in $J_{\mathrm{cg}}$ when $V_{\mathrm{g}}$ reached $-18.0$ V. The F–N tunneling current $J_{\mathrm{FNT}}$ owing to electrons passing through the blocking oxide film is written as

$$J_{\mathrm{FNT}} = \left(\frac{q^3 m}{8\pi h \Phi_b m_{\mathrm{ox}}}\right) {E_{\mathrm{box}}}^2 \exp\left(-\frac{4\sqrt{2m_{\mathrm{ox}}}{\Phi_b}^{3/2}}{3q\hbar E_{\mathrm{box}}}\right), \qquad (2)$$

where $m_{\mathrm{ox}}$ and $m$ are the electron masses in $SiO_2$ and in free space, respectively, $h$ is the Planck constant, $\hbar$ is the reduced Planck constant, and $\Phi_b$ is the energy barrier height of the blocking oxide film for electrons. $E_{\mathrm{box}}$ is the electric field in the blocking oxide film, which is written as [27]

$$E_{\mathrm{box}} = -\frac{V_{\mathrm{g}} - \phi_{\mathrm{ms}}}{t_{\mathrm{eq}}} + \Delta E_{\mathrm{hole}} + \Delta E_{\mathrm{fix}} \qquad (3)$$

where $t_{\mathrm{eq}}$ is the equivalent-oxide thickness of the stacked dielectric films, $\phi_{\mathrm{ms}}$ is the metal-semiconductor work function deference, $\Delta E_{\mathrm{hole}}$ is the electric field in the blocking oxide film caused by $Q_{\mathrm{trap}}(t_0,\ t_1)$, $\Delta E_{\mathrm{fix}}$ is the electric field in the blocking oxide film caused by the fixed positive charge. $\Delta E_{\mathrm{hole}}$ and $\Delta E_{\mathrm{fix}}$ are expressed as

$$\Delta E_{\mathrm{hole}} = -\frac{t_{\mathrm{tn}} + \frac{\varepsilon_{\mathrm{box}}}{\varepsilon_{\mathrm{ctl}}}(t_{\mathrm{ctl}} - \overline{x}_t)}{t_{\mathrm{eq}}} \cdot \frac{\Delta V_{\mathrm{fb,h}}}{t_{\mathrm{box}} + \frac{\varepsilon_{\mathrm{box}}}{\varepsilon_{\mathrm{ctl}}}\overline{x}_t} \qquad (4)$$

and

$$\Delta E_{\mathrm{fix}} = -\frac{t_{\mathrm{tn}} + \frac{\varepsilon_{\mathrm{box}}}{\varepsilon_{\mathrm{ctl}}}(t_{\mathrm{ctl}} - \overline{x}_{\mathrm{fix}})}{t_{\mathrm{eq}}} \cdot \frac{V_{\mathrm{fb,0}} - \phi_{\mathrm{ms}}}{t_{\mathrm{box}} + \frac{\varepsilon_{\mathrm{box}}}{\varepsilon_{\mathrm{ctl}}}\overline{x}_{\mathrm{fix}}}, \qquad (5)$$

where $\overline{x}_t$ is the charge centroid of $Q_{\mathrm{trap}}(t_0,\ t_1)$ measured from the SiCN-blocking oxide interface, $t_{\mathrm{tn}}$ is the thicknesses of the tunnel oxide film, $t_{\mathrm{ctl}}$ is the thicknesses of the charge trap layer, $t_{\mathrm{box}}$ is the thickness of the blocking oxide film, $\varepsilon_{\mathrm{ctl}}$ and $\varepsilon_{\mathrm{box}}$ are the relative dielectric constants of the charge trap layer and blocking oxide film, respectively. Then, $J_{\mathrm{FNT}}$ was computed by equations (2), (3), (4) and (5) using $V_{\mathrm{fb,0}}$ and $\Delta V_{\mathrm{fb,h}}$ determined from the C–V characteristics, the relevant parameter values listed in Table 1 and $\overline{x}_t$ as a fitting parameter.

Figure 6 shows the relationship between the absolute value of the gate current density $|J_{\mathrm{g}}|$ and $V_{\mathrm{g}}$ in the OCO memory capacitor. Assuming that neither trapped holes nor fixed positive charge exists in the stacked films and $\Delta E_{\mathrm{hole}} = \Delta E_{\mathrm{fix}} = 0$, the ideal F–N tunneling current of electrons through the blocking oxide film was calculated by

**Table 1.** The relevant parameter values used in the computation of the F–N tunneling current $J_{FNT}$. $\Phi_b = 3.4$ eV, which was estimated from the work function of aluminum (4.28 eV) [28] and the energy of the conduction band bottom in $SiO_2$ [29], and $\phi_{ms} = -0.63$ V, obtained from the Fermi level of the silicon substrate and the aluminum work function.

| Parameters relevant to OCO capacitors | | References |
|---|---|---|
| $V_{fb,0}$ | –3.4 V | |
| $t_1$ | 850 s | |
| $\Delta V_{fb,h}$ | –10.4 V | |
| $V_{g1}$ | –18.0 V | |
| $\varepsilon_{box}$ | 3.9 | |
| $\varepsilon_{ctl}$ | 4.8 | |
| $m_{ox}/m$ | 0.42 | [30] |
| $\Phi_b$ | 3.4 eV | [28,29] |
| $\phi_{ms}$ | –0.63 V | [29] |

equations (2) and (3) (dashed line). The coordinates $(V_{g1}, |J_{cg}|) = (-18.0\,\text{V}, 4.2\times10^{-9}\ \text{A/cm}^2)$ on the graph (filled square) was obtained from the experimental result shown in Figure 3. As explained in the previous paragraphs, $J_{cg}$ at a gate voltage of −18.0 V is dominated by $J_{FNT}$, which can be computed by equations (2), (3), (4) and (5). As shown by the dashed-dotted line in Figure 6, the computed $J_{FNT}$–$V_g$ curve was fitted to the coordinates $(V_{g1}, |J_{cg}|)$ with $\overline{x}_t$ of 1.8 nm and the parameters listed in Table 1. Thus, $\overline{x}_t$ of trapped holes has been determined to be 1.8 nm using a set of the $V_{g1}$ and $J_{cg}$ values.

The $J_g$–$V_g$ characteristics of the OCO stacked films was measured under negative gate bias after the constant-current carrier injection and is shown in Figure 6 (open circle). In this measurement, the gate voltage was stepped by 0.1 V every 61 s (delay time of 60 s) to prevent from detecting both the displacement current components induced by hole accumulation at the silicon surface and hole trapping in the SiCN layer. Therefore, the leakage current component is the dominant part in the measured gate current. The measured $J_g$–$V_g$ characteristics passes through the coordinates $(V_{g1}, |J_{cg}|)$ and is in good agreement with the fitted F–N tunneling current $J_{FNT}$ (dashed-dotted line). This fact supports that the F–N tunneling of electrons is the dominant mechanism of the charge transport across the stacked films at negative high gate voltages.

Next, the CCCI method presented in reference [26] was also used to obtain $\overline{x}_t$ values from $F_{inj}$ and $\Delta V_{fb,h}$ values ranging from −2.6 to −7.3 V shown in Figure 5. Figure 7 shows $\overline{x}_t$'s of holes trapped in the SiCN and silicon nitride charge trap layers as a function of $F_{inj}$. The relationship between $\overline{x}_t$ of holes trapped in the silicon nitride layer and $F_{inj}$ has been referred to from reference [27]. $\overline{x}_t$'s were initially located near the middle of the SiCN and silicon nitride layers and gradually moved toward the blocking oxide-charge trap layer interface as $F_{inj}$ increased. Finally, $\overline{x}_t$'s in the SiCN and silicon nitride layers reached 1.8–2.0 and 2.8–3.0 nm, respectively. Holes injected from the silicon substrate are transported due to the Poole-Frenkel conduction toward the interface under negative gate bias. In addition, some of holes captured once by trap sites are emitted from the sites due to the electric field generated by negative gate bias and are transported toward the interface [26]. The change of $\overline{x}_t$ shown in Figure 7 would be due to these mechanisms.

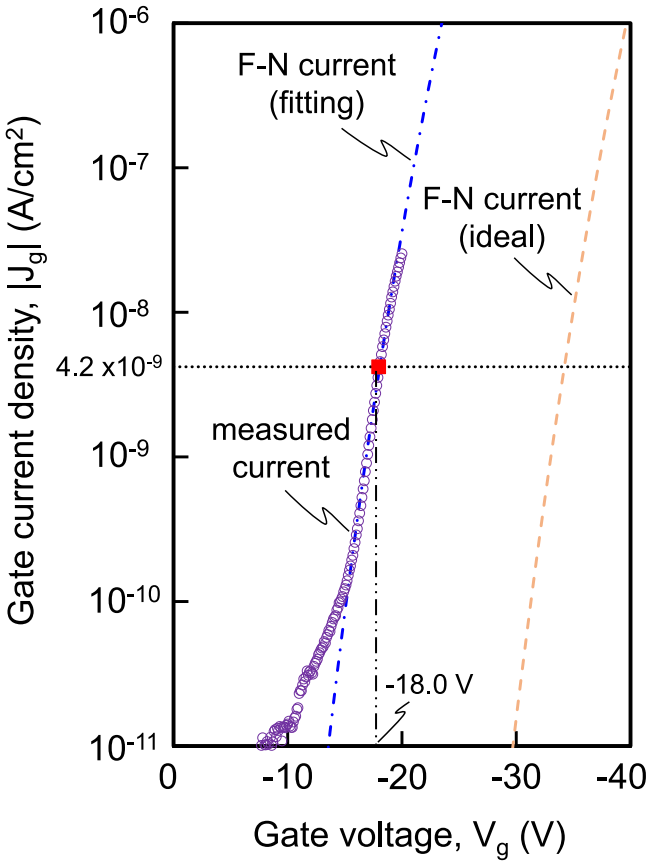


**Fig. 6.** Relationship between the absolute value of the gate current density $|J_g|$ and $V_g$ in the memory capacitor with the OCO stacked films. The coordinates $(V_{g1}, |J_{cg}|) = (-18.0\,\text{V}, 4.2\times10^{-9}\ \text{A/cm}^2)$ on the graph (filled square) is obtained from the experimental result shown in Figure 3.

The number of trapped holes per unit area $N_{trap}$ was calculated by the following equation:

$$N_{trap} = -\frac{\Delta V_{fb,h}}{q\left(\frac{t_{box}}{\varepsilon_0\varepsilon_{box}} + \frac{\overline{x}_t}{\varepsilon_0\varepsilon_{ctl}}\right)} \quad (6)$$

and is shown in Figure 8 as a function of $F_{inj}$. $N_{trap}$'s in the SiCN and silicon nitride layers are identical to each other at relatively small $F_{inj}$'s. That is because almost all holes injected from the silicon substrate to the layers are captured by empty trap sites and $F_{inj}$ is approximately equal to $N_{trap}$. On the other hand, at large $F_{inj}$'s, $N_{trap}$ in the SiCN layer was estimated to be $1.2\times10^{13}$ holes/cm$^2$, which was higher than that in the silicon nitride layer ($=1.0\times10^{13}$ holes/cm$^2$). As shown in Figure 5, $\Delta V_{fb,h}$ in

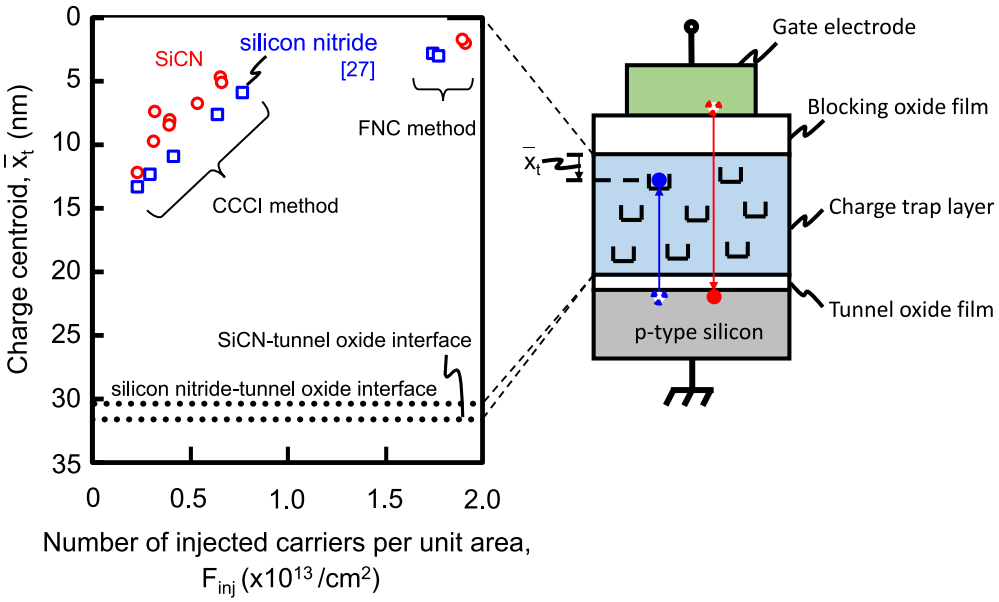


**Fig. 7.** Charge centroid $\overline{x}_t$ in two kinds of memory capacitors with the OCO and ONO stacked films as a function of $F_{\mathrm{inj}}$.

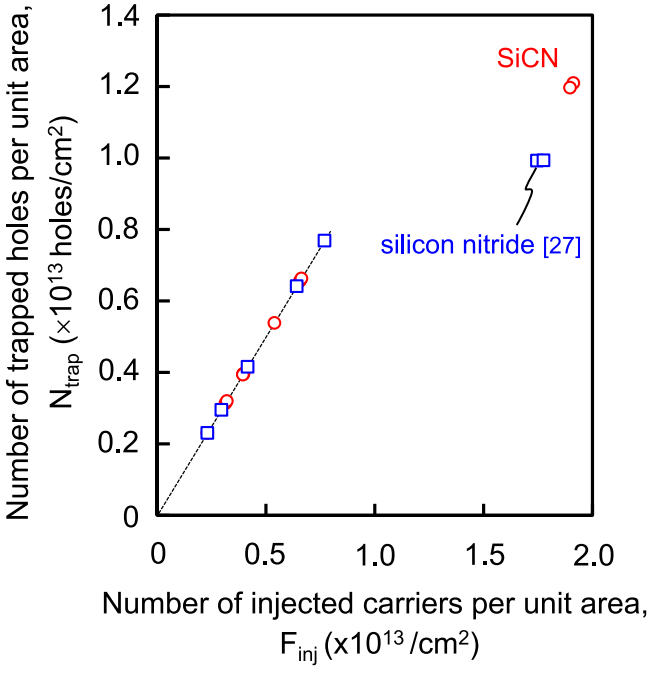


**Fig. 8.** Number of trapped holes per unit area $N_{\mathrm{trap}}$ in the SiCN and silicon nitride charge trap layers as a function of $F_{\mathrm{inj}}$.

the OCO structure at large $F_{\mathrm{inj}}$'s was about 1.2 times larger than that in the ONO structure. It is revealed that the high density of holes trapped in the SiCN layer is responsible for large $\Delta V_{\mathrm{fb,h}}$ in the OCO structure.

We have extracted $\overline{x}_t$ of holes trapped in the SiCN charge trap layer when $\Delta V_{\mathrm{fb,h}}$ in the OCO structure was saturated. Additionally, we have estimated the maximum density of holes trapped in the layer using the obtained $\overline{x}_t$ values. The OCO stacked films formed in this study was superior to the ONO stacked films in the hole trapping capability. The future-generation high-bit-density flash memories demand large flat-band voltage shifts to both positive and negative voltage directions to ensure sufficient reliability in terms of the data retention. The SiCN film with a high carbon content could be a potential candidate for the charge trap layer of them. As mentioned in Section 1, silicon dangling bonds were detected in high density in SiCN dielectric films [17–19]. The hole trap sites existing in the SiCN film might be attributable to silicon dangling bonds. However, since it has been reported that several kinds of point defects are present in silicon nitride films [31–35], the presence of several kinds of point defects in the SiCN film should be also assumed. To understand the reason for the superior hole trapping capability of the OCO stacked films, further studies on the origin of hole trap sites in the SiCN film would be needed.

## 4 Conclusions

The charge centroid $\overline{x}_t$ of holes trapped in the SiCN charge trap layer in MONOS-type memory capacitors has been determined using the method based on the analysis of F–N tunneling current of electrons through the blocking oxide film. The determination of $\overline{x}_t$ permitted us to estimate the maximum density of trapped holes. The number of trapped holes per unit area in the SiCN layer formed in this study was 1.2 times higher than that of the silicon nitride layer when the flat-band voltage shift $\Delta V_{\mathrm{fb,h}}$ was saturated at high applied voltages. It is concluded that the high density of holes trapped in the SiCN layer is responsible for large $\Delta V_{\mathrm{fb,h}}$ in the memory capacitors with the blocking oxide-SiCN-tunnel oxide stacked films. The SiCN film with a high carbon content has the potential to offer a solution for the charge trap material of future-generation flash memories.

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## Author contribution statement

All the authors were involved in the preparation of the manuscript. All the authors have read and approved the final manuscript.

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