Wide modulation bandwidth terahertz detection in 130 nm CMOS technology

Shamsun Nahar¹, Marwah Shafee², Stéphane Blin³, Annick Pénarier³, Philippe Nouvel³, Dominique Coquillat⁴, Amr M.E. Safwa², Wojciech Knap^{4,a}, and Mona M. Hella¹

¹ ECSE Department, Rensselaer Polytechnic Institute, Troy, NY 12180, USA

² ECE Department, Ain Shams University, 11566 Cairo, Egypt

³ Institut d'Électronique et des Systèmes, UMR 5214 CNRS-Université de Montpellier, 34095 Montpellier, France

⁴ Laboratoire Charles Coulomb (L2C), UMR 5221 CNRS-Université de Montpellier, 34095 Montpellier, France

Received: 11 August 2016 / Received in final form: 7 October 2016 / Accepted: 18 October 2016
© EDP Sciences 2016

Abstract. Design, manufacturing and measurements results for silicon plasma wave transistors based wireless communication wideband receivers operating at 300 GHz carrier frequency are presented. We show the possibility of Si-CMOS based integrated circuits, in which by: (i) specific physics based plasma wave transistor design allowing impedance matching to the antenna and the amplifier, (ii) engineering the shape of the patch antenna through a stacked resonator approach and (iii) applying bandwidth enhancement strategies to the design of integrated broadband amplifier, we achieve an integrated circuit of the 300 GHz carrier frequency receiver for wireless wideband operation up to/over 10 GHz. This is, to the best of our knowledge, the first demonstration of low cost 130 nm Si-CMOS technology, plasma wave transistors based fast/wideband integrated receiver operating at 300 GHz atmospheric window. These results pave the way towards future large scale (cost effective) silicon technology based terahertz wireless communication receivers.

1 Introduction

Recently, there has been an increased interest in terahertz (THz) and sub mm-wave systems for imaging and extreme wide bandwidth communications [1,2]. Being nearly unused, the frequency range starting from 280 GHz has no bandwidth-allocation limitations and therefore has the potential to allow ultra-fast data rates projected beyond 100 Gbps for short range communication applications [3]. A low cost, small form factor THz detector or receiver design is required to facilitate such applications, which could increase the use of the THz frequency range in everyday applications.

Existing THz detection technology includes thermal and optical based detectors such as bolometers, pyroelectric detectors, Golay cells, and Schottky barrier diodes (SBD) [4–6]. While thermal and optical detectors can operate over a wide frequency range with high responsivity and low noise performance, they are not suitable for a small form-factor integrated solution. Furthermore, the modulation frequency upper limit for most of these detectors lies in the kHz range, thus not useful for high speed imaging and wide band communication links.

Various coherent and incoherent semiconductor THz receivers have been proposed in silicon and III–V technologies [7–10]. In the published direct detection/incoherent systems, plasma wave field effect transistors (FETs) have been demonstrated as fast THz power detectors [11–21]. One important advantage of FET based THz detectors is that they are compatible with standard semiconductor integrated circuit (IC) technology and therefore can be used in the design and manufacturing of not only the detectors, but the whole receiver system in which the detector is followed by amplifiers and read-out circuitry [14,15,17].

The first circuits containing plasma wave detectors with amplifiers were manufactured mainly for imaging applications [14–16]. One has to stress that the requirements of THz wireless communications on the THz receiver circuitry are very different from those for imaging applications. In imaging applications, selective antennas with a narrow frequency band close to the THz beam frequency followed by the detector and low frequency (<MHz) narrowband amplifier are sufficient. For THz communications, the objectives are the data transfer in a Gbit/s range hence the signal modulation frequency should reach at least a few GHz range. Also the whole receiver (antenna, transistor and amplifier chain) should

^a e-mail: knap.wojciech@gmail.com

met a flat and very wide bandwidth (>10 GHz) conditions. In this case circuit integration is absolutely necessary because any impedance mismatch resulting from connections, like wire-bonding or even flip-chip bonding leads to parasitic resonances (not flat amplification band) and/or bandwidth limitations.

This has been shown by Blin et al. [20,21] who was the first to use single FET detectors for THz wireless communication. In these experiments, GaAs HEMTs were wire bonded to a $50\ \Omega$ printed circuit board (PCB) based transmission line followed by laboratory wideband amplifiers. These experiments have clearly shown that, the data rate transfer is limited to 8.2 Gbps by transistor and amplifier connections and that integrated receiver design is necessary to obtain a reduced size and cost effective communication module as well as push the data rate/bandwidth to the tens and potentially hundreds of Gbps rates.

While CMOS and SiGe technologies have been used for implementing communication transceivers up to 300 GHz [8–10] where an on chip antenna is followed by a down-conversion mixer and an intermediate frequency (IF) amplifiers, the power consumption for such receivers exceeded 200 mW depending on the operating frequency range and the used technology node.

To the authors' knowledge, this work represents the first characterization of FET detectors connected to wide-band integrated amplifiers in Si technology for THz wireless communication receivers. The complete wide band THz receiver IC, operating at 300 GHz carrier frequency and having 10 GHz bandwidth is fabricated using standard low cost 130 nm Si-CMOS technology and consumes only 45 mW of DC power.

The paper is organized as follows: Section 2 introduces the receiver architecture and related design considerations. Section 3 describes the detailed design of the basic building blocks. The measurement setup and results for low and high modulation frequencies are discussed in Section 4. Finally, conclusions are drawn in Section 5.

2 FET based THz detection

First proposed by Dyakonov and Shur, the operation principle of plasma-wave detectors has been explained using the shallow water analogy to the two dimensional electron fluid in FET channel [22]. It has also been described as a distributed self mixing resistive mixer [23] and by a lumped element approach for the region where the induced AC current exists [24]. A complete analytical expression valid in all regions of operation of the FET including sub-threshold, linear and saturation as well as the loading effect has been proposed in references [25,26]. Several detector designs for imaging applications employing on-chip antennas coupled to single ended and differential plasma-wave FET have been reported in Silicon and III–V technologies [11–19]. Low frequency on-chip amplification following the detector has been added to improve the overall responsivity [14,15,17]. Plasma wave detectors have also been recently reported for wide bandwidth communications in the THz regime. The FET detector can be

Fig. 1. (a) Plasma-wave FET operating regions [22,25], (b) calculated parameters for Si FETs at room temperature at a typical V_{ov} of 0.1 V, indicating that the detectors in this work operate in the low frequency long gate region, (c) critical length vs. overdrive voltage, L_0 does not exceed 120 nm even for a maximum V_{ov} of 0.8 V. The red dots refers to the calculated L_0 at 0.05 V and 0.25 V (the bias points considered in this work).

modulated at high frequencies depending on the applied gate bias voltage and the used channel length [27]. As mentioned in Section 1, Blin et al. [20,21] have demonstrated the potential of such applications by successfully detecting data rates up to 8.2 Gbps data using discrete GaAs transistors. However, this has not been yet demonstrated in an integrated solution. The important advantage of FET based THz detectors is the fact that the detector output impedance can be tuned by changing the gate bias voltage, thus providing an extra degree of freedom in interfacing with high or low impedance circuits elements based on the target application.

As shown in reference [25], the basic modes of FET based THz detectors can be classified into four groups (Fig. 1a). Plasma wave detectors can operate in a resonant or non-resonant, long or short channel modes depending on the channel length, the operating temperature and technology parameters such as electron carrier density and momentum relaxation time (τ), gate capacitance, and channel conductivity [22,25]. The plasma wave FET can also operate in a high frequency regime for operating frequencies higher than the critical frequency (f_c) defined in Figure 1b. Furthermore, if the device length is shorter than the high frequency critical length (L_H), the plasma wave FET operates in a resonant short gate mode and can detect specific THz frequencies depending on the gate bias and channel length. It is worth noting that as the temperature decreases, the mobility in Si increases, and the resonant mode could still be observed in relatively longer channels. However, in this work, only the room

temperature operation of transistors with gate length above 100 nm is considered. Thus, for a typical room temperature mobility (μ_0) of 300 cm²/V s in Si FETs, the CMOS detector can only operate in the low frequency regime for 300 GHz radiations (Fig. 1b). In this regime, plasma waves do not exist and the detector operates in the so-called overdamped plasma regime.

The critical length (L_0) is defined as the useful channel length that contributes to the plasma-wave or the distributed self-mixing based detection [28] and is calculated as:

$$L_0 = \sqrt{\frac{\mu_0 V_{ov}}{\omega}}, \quad (1)$$

where, ω is the operating angular frequency, μ_0 is the electron mobility and V_{ov} ($= V_{gs} - V_{th}$) is the overdrive voltage for the open channel conditions. V_{ov} is equal to thermal voltage multiplied by the ideality coefficient in the threshold and sub-threshold ranges, calculated to be 40 mV in this operating region. Therefore, L_0 remains constant in the subthreshold range and then increases with increasing V_{gs} for $V_{gs} > V_{th}$. L_0 is calculated for different overdrive voltages V_{ov} at 300 GHz. For low and high modulation frequency characterization, the FET detector has been biased at V_{ov} of 0.05 V and 0.25 V respectively. The critical lengths for a wide range of overdrive voltages spanning the weak inversion to the strong inversion regime is shown in Figure 1c. From the figure, $V_{ov} = 0.05$ V and 0.25 V corresponds to a critical length of 30 nm and 65 nm respectively. Thus, at room temperature, the minimum gate length (120 nm) for the CMOS FET in the used 130 nm CMOS technology can only allow non-resonant long channel THz detection.

In the non-resonant long channel mode of operation, the detector response depends on the gate and drain biasing, detector sizing and load impedances of the output circuitry as shown in Figure 2a. Depending on the drain bias voltage or current, the detector operates in either an open drain (no DC drain current) or current-driven (drain biased at a constant current) mode. In the open drain mode, the response can be described as [26]:

$$R_v = A \frac{d}{dV_{gs}} \ln(g_{ch}), \quad (2)$$

$$R_{vl}(\text{open drain}) = \frac{A}{1 + R_{ch}/Z_L} \frac{d}{dV_{gs}} \ln(g_{ch}) \quad (3)$$

$$= A * A_L * \frac{d}{dV_{gs}} \ln(g_{ch}),$$

where A is a constant representing the incident signal amplitude and accounts for the antenna efficiency and mismatch loss, R_{ch} is the channel resistance, Z_L is the load resistance, $A_L = 1/(1 + R_{ch}/Z_L)$ is the loading factor, $g_{ch} = 1/R_{ch}$ is the channel conductance. Since the contact resistance is much smaller than the load impedance (Z_L) for the device operating conditions considered here, it has not been included in the above expression for A_L . The voltage response (R_v) is inversely proportional to g_{ch} and thus to the gate overdrive voltage, $V_{ov} = V_{gs} - V_{th}$. Therefore, for the open load condition ($Z_L \approx \infty$), R_v

Fig. 2. (a) The equivalent circuit model of the THz FET detector, (b) detector output voltage and loading factor (inset) vs. gate bias voltage at different load impedances. The load impedance (Z_L) has been chosen to be multiple/fraction of the channel resistance at the device threshold voltage ($R_{ch,vth}$). The peak R_{vl} increases with increasing the load impedance. The given values are calculated from a typical FET I-V characteristics ($V_{th} = 0.2$ V) using 130 nm CMOS technology parameters.

remains constant for $V_{gs} < V_{th}$ and rolls off with increasing V_{ov} as shown in Figure 2b.

To explain the loading effect on the detector response, the detector can be modeled as a voltage source with a source resistance of R_{ch} in series with the input impedance of the read out circuitry or the amplifier (Fig. 2a). As shown in Figure 2b, R_{vl} rolls off at lower V_{gs} due to the loading effect ($R_{ch} \gg Z_L$), peaks when the multiplication of the two functions reaches maximum and then rolls off again due to the inverse relationship with V_{gs} . Thus, the detector response is the highest for the maximum possible R_{ch} i.e., when biased near V_{th} and for $Z_L \gg R_{ch}$.

The above operating condition can be achieved in applications where the incident radiation source is modulated with a low modulation frequency source such as a chopper stage. However, as the modulation frequency increases, the interface between the detector and the on-chip amplifier becomes critical as the output impedance of the detector interfaces with the input impedance of the on-chip amplifier and controls the maximum bandwidth achieved for the THz detection chain. To achieve a higher bandwidth, the FET detector needs to be biased and sized for a lower R_{ch} . Also, the input capacitance of the following amplification circuit needs to be as low as

Fig. 3. Receiver block diagram and schematic of the designed wide band amplifier stages. The design dimensions are: $(W/L)_{M_{1,2,3,4}} (\mu\text{m}/\mu\text{m}) = 16/0.12$, $(W/L)_{M_{5,6}} (\mu\text{m}/\mu\text{m}) = 18/0.12$, $(W/L)_{M_{7,8}} (\mu\text{m}/\mu\text{m}) = 2.5/0.12$, $R_{L1} = 150 \Omega$, $R_{L2,4} = 250 \Omega$, $R_{L3} = 300 \Omega$, $L_d = 0.8 \text{ nH}$, $(W/L)_{M_{9,10,11,12}} (\mu\text{m}/\mu\text{m}) = 32/0.12$, $R_{LB} = 75 \Omega$, where W and L refers to the width and length of the transistors $M_{1...10}$.

possible so that the RC product at the interface is minimized. Such bias and loading condition would result in reduced responsivity as shown in Figure 2b.

When current is driven to the drain terminal (current-driven mode), the non-resonant, long channel plasma-wave response increases sharply due to the increased channel asymmetry as described in reference [29]. The current driven response (valid only in the triode region) can be given as:

$$R_{v1}(\text{current driven}) = \frac{A}{1 + R_{ch}/Z_L} \frac{1}{V_{ov} \sqrt{1 - j_d/j_{sat}}}, \quad (4)$$

where j_d and j_{sat} represent the drain current density at the triode and saturation regimes. Thus, the response increases significantly when the bias current approaches the saturation current. However, the channel resistance also increases by an order of magnitude from the triode to the saturation regions, thus narrowing the bandwidth, while increasing the response. Therefore, the same response-bandwidth trade off exists both in open drain and current driven mode. Due to the $1/f$ noise contribution from the DC drain bias current, the detector noise contribution also increases compared to the open drain operation mode and the signal to noise ratio stays the same.

3 THz receiver design

The chip is designed and fabricated in IBM 130 nm CMOS technology. The technology includes eight metal layers with a metal stack height of $16 \mu\text{m}$. The detailed receiver block diagram is shown in Figure 3. The chip consists of a stacked half wave patch antenna connected at the gate terminal of the plasma-wave detector followed by a wide

band on-chip amplifier. The amplifier is connected at the FET's drain terminal through a 1.5 pF on-chip dual metal-insulator-metal (MIM) capacitor as DC blocking capacitor. The drain terminal is also connected to a bias pad through a $10 \text{ k}\Omega$ resistance to enable both open drain and current driven operating conditions.

3.1 On-chip enhanced bandwidth patch antenna

Bow-tie [13], dipole [14, 16, 18] and ring antennas [30] have been recently used for wide bandwidth THz detection. While having the wideband advantage, such structures couple a significant percentage of the radiation to the substrate and not to the FET detector terminals. This issue was addressed in details by Coquillat et al. [31]. In this design, we elected to use a regular patch antenna geometry where the ground plane blocks the parasitic substrate related losses. While patch antennas are usually narrow band, to improve the bandwidth, an additional patch with close resonance frequency is added. The antenna shown in Figure 4a consists of two vertically stacked resonators that are realized on the 7th and 8th top metal layers in the technology. The upper patch resonates at 300 GHz while the lower patch resonates at 292 GHz . The combined return loss is shown in Figure 4b, showing a bandwidth ($S_{11} < -10 \text{ dB}$) of 19 GHz .

The ground plane of the antenna is implemented using the lower metal layer (M1). To adhere to the technology design rules regarding the maximum metal width, narrow longitudinal slots parallel to the current directions are added (Fig. 4a). The lower patch resonates at the lower side of the frequency range. Thus, it has a longer electrical length than the upper patch. To decrease the physical length of the lower patch, a horizontal slot is also added.

Fig. 4. Wideband antenna using stacked resonators, (a) the design dimensions are; $L_{\text{patch}} = 235.6 \mu\text{m}$, $W_{\text{patch1}} = 260 \mu\text{m}$, $W_{\text{patch2}} = 160 \mu\text{m}$, $L_{\text{slot}} = 68.2 \mu\text{m}$, $W_{\text{slot}} = 5 \mu\text{m}$, $L_{M1_slot} = 90 \mu\text{m}$, $L_{M7_slot} = 40 \mu\text{m}$, feed line length and width are $120 \mu\text{m}$ and $14 \mu\text{m}$, respectively, inset distance and width are $30 \mu\text{m}$ and $5 \mu\text{m}$. (b) Return loss of the upper patch, lower patch, and the combined antenna.

The antenna's simulated fractional bandwidth (FBW) is 6.39%, which is almost three times that of a regular patch antenna [32]. The antenna gain is 1.26 dB and the radiation efficiency is 44.6% at 300 GHz.

3.2 THz FET-based detector and wide band amplifier

A triple well N channel MOSFET with a gate length of 120 nm and a width of $10 \mu\text{m}$, acts as a plasma-wave FET detector. As shown in Figure 1, the critical length (L_0) is calculated to be $<70 \text{ nm}$ for the V_{ov} in consideration. Thus, to minimize the parasitic loss contributed by the rest of the channel beyond the 70 nm length, the minimum gate length is selected. Since, the chip is designed for wide band applications specifically, the channel width is chosen as $10 \mu\text{m}$, which is wider than the minimum width allowed. The wider channel width minimizes R_{ch} , which in turn minimizes the loading at the interface of the detector and the on-chip amplifier.

The interface at the FET detector and the amplifier represents a design compromise between the achievable detector responsivity (signal to noise ratio) and bandwidth. The detector bias voltage and sizing is chosen to provide an R_{ch} of 300Ω at the amplifier input. With this

high source resistance, the input capacitance of the first stage needs to be as low as $\sim 25 \text{ fF}$ to obtain a 15 GHz overall bandwidth. To achieve that, a combination of f_t doubler, active feedback, and shunt peaking has been employed in the first stage [33,34]. In the f_t doubler circuit, the input signal is fed to a series combination of two FETs, thus halving the input capacitance. Shunt peaking and active feedback improve the achievable bandwidth by introducing a zero in the transfer function and minimizing the loading impedances at the interface of the cascaded stages respectively. The first stage also works as an active single ended to differential converter for the single ended output from the detector drain terminal. The subsequent four gain stages have a similar architecture employing active feedback and shunt peaking. The design parameters and device dimensions are shown in Figure 3.

The amplifier includes a buffer stage to interface with the 50Ω load. The buffer stage consists of an f_t doubler circuit without any inductive peaking. The buffer load resistance is selected as 75Ω to compensate for the channel length modulation effect and parasitics at the output pad.

4 Measurement results

4.1 Characterization of the antenna-coupled detector

The circuit schematic and die micrograph for the stand alone antenna coupled detector is shown in Figure 5. To characterize the behavior of the detector, the incoming radiation is chopped optically at a low modulation frequency (619 Hz) and the response signal is read using a synchronized lock in amplifier. The output of the detector is taken directly from through detector's drain terminal [35].

The measurement setup shown in Figure 5a, includes an amplifier/multiplier chain from Virginia Diodes, Inc. (model number VDI AMC 373) as electronic THz source. The THz source is tuned from 265 GHz to 375 GHz with an average power of 1 mW . The THz beam from the VDI AMC 373 is modulated using an optical chopper from Thorlabs (MC 2000 with 10 slot blades) and then collimated using two plane and four parabolic mirrors to have two focal points; the first for the object during imaging experiments (optional) and the second one for the detector circuitry. The receiver pads are wire bonded to side-brazed dual in-line ceramic packages (SBDIP) and the sample is mounted on an XYZ translation stage, which is used to align the receiver in the beam focal point. For responsivity calculation, the incident THz power and beam size at the detector plane is measured using absolute terahertz power/energy meter from Thomas Keating. The average power at the incident plane is measured as 0.35 mW with the beam profile shown in Figure 5b. For a gaussian profile, and considering a full width at the half maxima, the beam area is calculated as 13 mm^2 . The voltage response at the detector drain terminal is then measured using a lock-in amplifier (Signal Recovery 7265). The input impedance of the lock in amplifier and chopper frequency are set to $10 \text{ M}\Omega$ and 619 Hz respectively.

Fig. 5. (a) Circuit schematic, (b) die micrograph for the stand alone antenna coupled detector, (c) measurement setup using a THz source with low frequency modulation and (d) incident beam area calculation.

Fig. 6. Responsivity measured at a modulation frequency of 619 Hz (a) vs. frequency (b) vs. gate voltage for different drain bias current.

The antenna coupled detector is characterized for open drain and current driven modes. In the open drain mode, the responsivity peaks at a gate bias of 0.19 V near the threshold voltage of the FET (V_{th}) as explained in reference [25]. To measure the frequency response and the antenna bandwidth, the detector response is then measured within the frequency range of 265 GHz–375 GHz at a fixed gate bias voltage of 0.19 V. As shown in Figure 6a, the absolute responsivity peaks at 292 GHz with a bandwidth of 17 GHz that extends from 286 to 303 GHz. The measured result shows good agreement with the antenna simulation results (19 GHz from 287 to 306 GHz). In current driven mode, the detector response is measured for a drain bias current of 0 to 5 μ A. Though the frequency response remains unchanged, the absolute responsivity increases to ~ 30 V/W at a drain current of 5 μ A. The voltage dependence has also been measured for a fixed frequency (292 GHz) for a gate bias voltage

range of 0–0.8 V and a drain bias current of 0–5 μ A. The channel resistance (R_{ch}) increases with increasing the current and decreases with the over drive voltage (V_{ov}). Such measurement results confirm the model depicted in Figure 2a as the gate bias for peak responsivity increases with increasing the drain current (Fig. 6b).

Another parameter of interest is the area normalized responsivity, which is calculated using the following equation:

$$R_N = \frac{R_v}{P_{det}} = \frac{R_v A_{beam}}{P_{inc} A_{det}}, \quad (5)$$

where R_N is the area normalized responsivity in V/W, R_v is drain response voltage with a load impedance of Z_L , P_{det} is the power incident on the detector, A_{beam} is the incident beam area, P_{inc} is the total incident power with a beam area of A_{beam} and A_{det} is the antenna effective area. From Figure 5b, A_{beam} is 13 mm² and A_{det} is calculated

Fig. 7. Open drain NEP for different gate bias voltage. The reported NEP is calculated for absolute responsivity; the NEP would improve by a factor of ~ 56 for area normalized responsivity consideration.

using $\lambda^2 D_r / 4\pi$ [14] as 0.23 mm^2 for a simulated directivity of 4.7 dB; where D_r is the antenna directivity. Given the numbers above, the antenna coupled detector achieves an R_N of 2 kV/W at 292 GHz for the current driven mode.

The noise equivalent power (NEP) for the plasma wave detector for the open drain mode has been calculated using the following equation [11, 36]:

$$\text{NEP} = \frac{\sqrt{4KT(R_{\text{ch}} \| Z_L)}}{R}, \quad (6)$$

where, K is the Boltzmann's constant, T is the temperature, R_{ch} is the detector channel resistance, Z_L is the load resistance and R is either absolute or normalized detector responsivity. This equation assumes the channel resistance thermal noise is the dominant noise source in the open drain mode as demonstrated in reference [11, 36]. The channel resistance is derived from the measured I - V characteristic of the FET detector and the calculated NEP with absolute responsivity for different gate bias is shown in Figure 7. The antenna coupled detector achieves a minimum NEP of $10 \text{ nW}/\sqrt{\text{Hz}}$ and $175 \text{ pW}/\sqrt{\text{Hz}}$ for absolute and area normalized responsivity at a gate bias of 0.45 V.

4.2 Characterization with a high frequency modulated THz signal

To measure the bandwidth of the 300 GHz receiver, the complete circuit shown in Figure 3 is characterized using the setup shown in Figure 8a. In this experiment, a THz carrier signal at 292 GHz is mixed with a sinusoidal RF signal and used as the incident source signal. If the carrier and the RF signals are represented using $A_c \cos \omega_c t$ and $A_m \cos \omega_m t$ respectively, then the incident signal can be expressed as:

$$x_{\text{inc}}(t) = A_c \cos \omega_c t \times A_m \cos \omega_m t, \quad (7)$$

Fig. 8. (a) Measurement setup for high modulation frequency, (b) PCB and (c) die micrograph of the whole chip.

where A_c , A_m are the carrier and RF signal amplitudes and ω_c , ω_m are the carrier and RF signal angular frequency respectively. Now, according to the self-mixing resistive mixer [23] model of FET-based detector, the output at the detector can be expressed in a simplified form as the square of the input signal. Thus, the detector essentially works as a power detector. The output at the power detector can be expressed as:

$$\begin{aligned} x_{\text{out}}(t) &= (x_{\text{inc}})^2 = (A_c \cos \omega_c t \times A_m \cos \omega_m t)^2 \\ &= \frac{A_c^2 A_m^2}{4} (1 + \cos 2\omega_m t)(1 + \cos 2\omega_c t) \\ &= A_d (1 + \cos 2\omega_m t + \cos 2\omega_c t + \cos 2\omega_c t \cos 2\omega_m t), \end{aligned} \quad (8)$$

where A_d is a constant representing the amplitude of the demodulated signal. Therefore, as in equation (8), the demodulated RF signal is measured at twice the input RF signal. This is applicable only for carrier suppressed modulated signal. For amplitude modulated signals with modulation index ≤ 1 , the RF signal is demodulated at the same frequency range as in the input. Further experimentation with lower modulation index and random data generator is being carried on.

The setup for high frequency measurements is formed of a VDI multiplier chain followed by a second harmonic mixer (VDI 147 Rx). The $24\times$ multiplier chain up-converts the output signal of an external synthesizer (Rhode & Schwartz SMB100A) with a frequency tunability from 11.7 to 14.6 GHz. Thus, the carrier signal frequency can be changed from 280 to 350 GHz. The mixer multiplies the THz carrier signal with the incoming RF input from Agilent MXG N5183B. The power level of the external RF input is set to -5 dBm and the frequency can be varied from dc to 30 GHz. A horn antenna at the output of the mixer radiates the generated modulated THz signal with an average power of $20 \mu\text{W}$. The receiver die is wire bonded to a custom PCB. The PCB is designed with ROGERS 4003 material (R04003c) and achieves a bandwidth of 10 GHz. The THz signal from the horn

Fig. 9. Measurement results for modulation frequencies up to 20 GHz, (a) responsivity vs. frequency, (b) SNR vs. frequency for different drain bias currents.

antenna is collimated using a Teflon lens with a focal length of 10 cm and then focused using another Teflon of the same focal length on the translational stage holding the PCB. The differential output from the amplifier is converted to a single ended signal using an external wide band balun (Hyperlab HL9402 Balun) and measured using a spectrum analyzer (Rhode & Schwartz FSU). The measurement setup along with the die micrograph and the printed circuit board (PCB) is shown in Figure 8.

The measured responsivity with and without the drain bias current is shown in Figure 9a. The gate bias of the plasma wave detector is kept fixed at 0.4 V to minimize the loading effect when interfacing with the on-chip amplifier. As can be seen in Figure 9a, 5 times improvement is achieved by introducing the drain bias current. The bandwidth for the open drain and current driven modes is measured to be 10 and 3.5 GHz respectively. The reduction in bandwidth is due to the increased channel resistance and subsequent loading of the first stage of the amplifier. The response above 10 GHz is limited by the PCB bandwidth. The receiver noise performance is also included in Figure 9b. For the signal to noise ratio (SNR) measurement, the noise has been recorded in the same setup shown in Figure 8 with the THz source turned off and the integrated chip set to the same bias conditions as it was while measuring the responsivity. The noise is recorded in the spectrum analyzer for a resolution bandwidth of 3 Hz. The SNR is then calculated from the recorded voltage response and noise data. The measured noise includes the circuit noise as well as the environmental noise since no anechoic chamber or EM shielding has been used during the measurements. The receiver maintains a minimum 40 dB SNR over the 10 GHz band for both the operating modes. The fabricated receiver consumes 45 mW of dc power.

5 Conclusion

FET detector based imaging systems have been extensively researched with published results showing the

potential for efficient images having minimal area, low dc power consumption and the possibility of integration in mainstream CMOS technologies. Its application as a wide band THz detector for ultra wide band short range communication is yet to be validated. While offering the same low cost, low power, low form factor option, wide band FET detection needs to address several design challenges including optimum bias condition, interfacing with on or off chip amplification and on-chip antenna bandwidth enhancement. In this paper, a fully integrated antenna-detector-wideband amplifier chip is presented at 300 GHz with 10 GHz measured bandwidth (limited by the printed circuit board). In the open drain and current driven modes, the receiver achieves an absolute responsivity of 4 V/W and 20 V/W with 10 GHz and 3.5 GHz bandwidth respectively. The measured noise performance shows a SNR above 40 dB for the entire bandwidth in both modes of operation.

This work is partially supported by the SRC and the Texas Analog Center of Excellence (TxACE) under task number 1836.079 and the National Science Foundation award number IIP-1445042. This work was also partially supported by the National Center for Research and Development in Poland grant PBS1/A9/11/2012 and by the ANR P2N NADIA Integrated NANO-Detectors for terahertz Applications (ANR-13-NANO-0008). The authors acknowledge MOSIS support for fabrication.

References

1. C. Jansen, S. Wietzke, O. Peters, M. Scheller, N. Vieweg, M. Salhi, N. Krumbholz, C. Jördens, T. Hochrein, M. Koch, *Appl. Opt.* **49**, E48 (2010)
2. I.F. Akyildiz, J.M. Jornet, C. Han, *Physical Communication* **12**, 16 (2014)
3. T. Kurner, [Online]. <http://www.ftw.at/events/telecommunications-forum/thz-communications-an-option-for-wireless-100-gbps>
4. Microtech Instruments. [Online] <http://www.mtinstruments.com/downloads/Pyroelectric>

5. Tydex Optics. [Online] <http://www.tydexoptics.com/pdf/Golaycell.pdf>
6. Infrared Laboratories. [Online] <http://www.infraredlaboratories.com/uploads/IRLabs-Bolometers-WEB.pdf>
7. Y. Zhang, R. Han, Y. Kim, D.Y. Kim, H. Shichijo, S. Sankaran, M. Chuying, S. Eunyong, D. Shim, K.O. Kenneth, in *2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, *IEEE EXpress Conference, New York, 2013*, pp. 24–26
8. S.V. Thyagarajan, K. Shinwon, A.M. Niknejad, in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, *IEEE EXpress Conference, New York, 2014*, pp. 357–360
9. J.-D. Park, S. Kang, S.V. Thyagarajan, E. Alon, A.M. Niknejad, in *IEEE Symposium on VLSI Circuits (VLSIC)*, *IEEE EXpress Conference, New York, 2012*, pp. 48–49
10. E. Ojefors, B. Heinemann, U.R. Pfeiffer, *IEEE Trans. Microwave Theor. Tech.* **60**, 1397 (2012)
11. R. Tauk, F. Teppe, S. Boubanga, D. Coquillat, W. Knap, Y.M. Meziani, C. Gallon, F. Boeuf, T. Skotnicki, C. Fenouillet-Beranger, D.K. Maude, S. Rummyantsev, M. Shur, *Appl. Phys. Lett.* **89**, 253511 (2006)
12. S. Boppel, A. Lisauskas, M. Mundt, D. Seliuta, L. Minkevicius, I. Kasalynas, G. Valusis, M. Mittendorff, S. Winnerl, V. Krozer, H.G. Roskos, *IEEE Trans. Microwave Theor. Tech.* **60**, 3834 (2012)
13. F. Schuster, H. Videlier, A. Dupret, D. Coquillat, M. Sakowicz, J. Rostaing, M. Tchagaspian, B. Giffard, W. Knap, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, *IEEE EXpress Conference, New York, 2011*, pp. 42–43
14. E. Ojefors, U. Pfeiffer, A. Lisauskas, H. Roskos, *IEEE J. Solid-State Circuits* **44**, 1968 (2009)
15. E. Ojefors, N. Baktash, Y. Zhao, R. Hadi, H. Sherry, U. Pfeiffer, in *Proceedings of the ESSCIRC*, *IEEE EXpress Conference, New York, 2010*, pp. 486–489
16. H. Sherry, R. Al Hadi, J. Grzyb, E. Ojefors, A. Cathelin, A. Kaiser, U. Pfeiffer, in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, *IEEE EXpress Conference, New York, 2011*, pp. 1–4
17. U. Pfeiffer, E. Ojefors, in *34th European Solid-State Circuits Conference (ESSCIRC)*, *IEEE EXpress Conference, New York, 2008*, pp. 110–113
18. R. Al Hadi, H. Sherry, J. Grzyb, N. Baktash, Y. Zhao, E. Ojefors, A. Kaiser, A. Cathelin, U. Pfeiffer, in *IEEE MTT-S International Microwave Symposium (IMS)*, *IEEE EXpress Conference, New York, 2011*, pp. 1–4
19. S. Nahar, A. Gutin, A. Muraviev, I. Wilke, M. Shur, M.M. Hella, in *IEEE MTT-S International Microwave Symposium (IMS)*, *IEEE EXpress Conference, New York, 2014*, pp. 1–4
20. S. Blin, L. Tohme, D. Coquillat, S. Horiguchi, Y. Minamikata, S. Hisatake, P. Nouvel, T. Cohen, A. Pénarier, F. Cano, L. Varani, W. Knap, T. Nagatsuma, *J. Comm. Networks* **15**, 559 (2013)
21. L. Tohme, G. Ducournau, S. Blin, D. Coquillat, P. Nouvel, A. Penarier, W. Knap, J.F. Lampin, in *38th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, *IEEE EXpress Conference, New York, 2013*, p. 1
22. M. Dyakonov, M. Shur, *IEEE Trans. Electron Devices* **43**, 380 (1996)
23. A. Lisauskas, U. Pfeiffer, E.O. Ojefors, G. Haring, R. Diana, G. Hartmut, *J. Appl. Phys.* **105**, 114511 (2009)
24. S. Preu, K. Sangwoo, R. Verma, P.G. Burke, N.Q. Vinh, M.S. Sherwin, A.C. Gossard, *IEEE Trans. Terahertz Sci. Technol.* **2**, 278 (2012)
25. W. Knap, M. Dyakonov, D. Coquillat, F. Teppe, N. Dyakonova, J. Lusakowski, K. Karpierz, M. Sakowicz, G. Valusis, D. Seliuta, I. Kasalynas, A. El Fatimy, Y.M. Meziani, T. Otsuji, *J. Infrared Millim. Terahertz Waves* **30**, 1319 (2009)
26. M. Sakowicz, M.B. Lifshits, O.A. Klimenko, F. Schuster, D. Coquillat, F. Teppe, W. Knap, *J. Appl. Phys.* **110**, 054512 (2011)
27. V. Kachorovskii, M. Shur, *Solid-State Electron.* **52**, 182 (2008)
28. A. Gutin, S. Nahar, M. Hella, M. Shur, *IEEE Trans. Terahertz Sci. Technol.* **3**, 545 (2013)
29. D. Veksler, F. Teppe, A. Dmitriev, V. Kachorovskii, W. Knap, *Phys. Rev. B* **73**, 125328 (2006)
30. M. Uzunkol, J.M. Edwards, G.M. Rebeiz, in *2014 IEEE MTT-S Int. Microw. Symp. (IMS)*, *IEEE EXpress Conference, New York, 2014*, pp. 1–4
31. D. Coquillat, J. Marczewski, P. Kopyt, N. Dyakonova, B. Giffard, W. Knap, *Opt. Express* **24**, 272 (2016)
32. M. Shafee, S. Nahar, A. Safwat, H. El-Hennawy, M.M. Hella, in *IEEE International Conference on Ultra Wide Band*, *IEEE EXpress Conference, New York, 2014*, pp. 240–244
33. S. Galal, B. Razavi, *IEEE J. Solid State Circuits* **38**, 2138 (2003)
34. B. Razavi, *Design of Integrated Circuits for Optical Communications*, 2nd ed., (Wiley, New Jersey, 2012), pp. 130–171
35. A. Zolfaghari, A. Chan, B. Razavi, in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, *IEEE EXpress Conference, New York, 2000*, pp. 345–348
36. F. Schuster, D. Coquillat, H. Videlier, M. Sakowicz, F. Teppe, L. Dussopt, B. Giffard, T. Skotnicki, W. Knap, *Opt. Express* **19**, 7827 (2011)