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An accurate SPICE-compatible circuit model for power FLYMOSFETs

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Abstract. In this paper, a new SPICE-compatible circuit model for low voltage, low on-resistance power FLYMOSFETs is presented for the first time. In this new structure, the improvement of the on-resistance has been obtained by inserting floating islands in the lowly doped layer. Our modelling is based on device physics, analytical study and on experimental characterization. The inter-electrode capacitances are modelled accurately as nonlinear functions, and good agreement between simulation and measurements is found.

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1 Introduction

Power MOSFET is a commonly used power device in many power electronics applications, in the voltage range below 600 Volts, for its well-known intrinsic advantages: high input impedance, short switching time and thermal stability. Unfortunately, the specific on-resistance ($R_{ON}.S$) of power MOSFET increases drastically with the increase of its breakdown voltage (V_{br}). Due to the limitation of the maximum electric field, a high breakdown voltage requires the drift region to be lightly doped and large, which in turn causes $R_{ON}.S$ to be very high. The theoretical limit, called "Silicon limit", of the "$R_{ON}.S$ / V_{br}" trade-off of conventional vertical power MOSFETs is given by the relationship [1]:

$$R_{ON}.S(\Omega.\text{cm}^2) = 8.3 \times 10^{-9} \times (V_{br})^{2.5}. \qquad (1)$$

Nowadays the Vertical Double diffused MOSFET structure — VDMOSFET — (Fig. 1) is widely used as a power MOSFET. This structure is based upon the double diffusion of the P-body and N^+ source regions using the edge of the polysilicon as a masking boundary. The voltage handling capability of this structure is given by the breakdown voltage of the "P-body / N^- epilayer" junction, that is strongly dependent on the thickness and the doping of the lower doped region (i.e. the N^- epilayer region in the case of N-channel VDMOS transistors) [1]. Today, advances in process technology have improved transistor's packing density and, consequently, transistor's specific on-resistance. However improvements in specific on-resistance have been limited by material and breakdown voltage, which required a relative thick and lowly doped epitaxial layer.

Recently, several MOSFET configurations have been proposed to reduce specific on-resistance while keeping a high breakdown voltage: P-floating islands devices [2–4] and Superjunction devices [5]. P FLoating Islands unipolar devices — FLIMOSFET [2], Opposite Doped Buried Regions (ODBR) MOSFET [3] and P-buried layer Schottky Barrier Diode [4] — have recently caught the attention of many researchers because they are good challengers of Superjunction devices under 600 Volts breakdown voltage [2]. Furthermore, the "Floating Islands" concept is not based on the charge compensation principle unlike the Superjunction concept [5]: then the technology needed to manufacture such devices is less complex than the Superjunction devices technology.

The FLYMOSFET (or FLIMOSFET) was recently proposed by Cézac et al. [2] to reduce the specific on-resistance by inserting a floating island in the lightly doped region (Fig. 2). The specific on-resistance is improved by the increase in the doping level of the drift region (N^- epitaxial layer) compared to a conventional VDMOSFET with the same breakdown voltage. However, this increase in the doping concentration of the drift region can affect the feedback capacitance C_{gd} and drain to source capacitance C_{ds} of the device.

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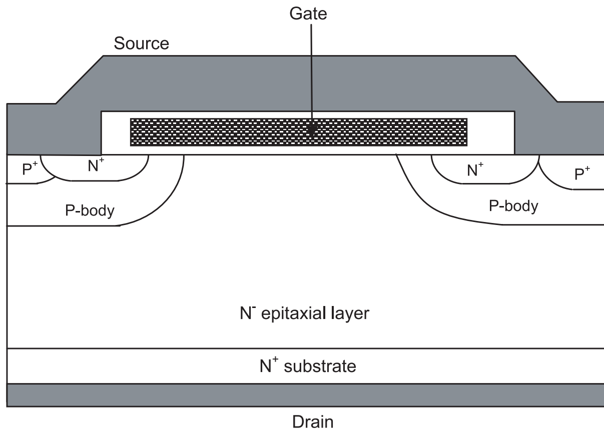

Fig. 1. Cross section of a cell of the conventional power Vertical DMOSFET.

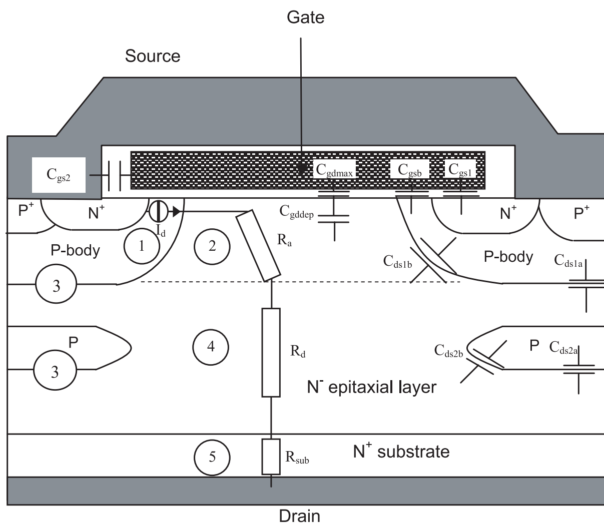

Fig. 2. Cross-section of a cell of the power Vertical FLYMOSFET with one P-floating buried layer between drain and source and location of some items in the complete model.

Concerning circuit modelling of power MOSFETs, a lot of research works have been recently done [6–9] but no modelling of the power FLYMOSFET was done to date. In this paper, a new SPICE-compatible circuit model of a low voltage (65 Volts), low on-resistance (2 mΩ) power FLYMOSFET is presented for the first time. This circuit model is based on device physics, analytical study, measurements and ATLAS (by SILVACO) simulations [10]. Our modelling approach is very simple, employs existing MOS models and yet still provides accurate results. Furthermore, this new model describes many unique properties of power FLYMOSFETs using arguments based on familiar MOS theory and on the physical structure of the devices.

In the following sections, we describe the new circuit model, explain its physical foundations and compare this model with measured data for a 65 Volts FLYMOSFET.

2 Basic principle of operation

Schematic cross-sections of the conventional Vertical DMOSFET (VDMOSFET) and the newly developed Vertical FLYMOSFET are shown in Figures 1 and 2. In the conventional structure, the N^- drift region is required to be lightly doped so that the depletion region sufficiently develops in this region to sustain the blocking voltage. This lightly doped N^- drift region results in a high drift resistivity. The FLYMOS transistor structure is characterized by the introduction of a P-buried floating layer (called FLoating Island) in the N^- epitaxial region; this P-buried layer, located under the "P-body / N^- drift" plane junction, enhances the development of depletion layer due to the similar mechanism of P-guard rings in planar terminations, i.e. once the depletion region from the source side reaches the P-buried floating layer, the voltage of the layer is pinned due to punch-through between the floating layer and the P-body; then new depletion layer develops from the bottom of the P-floating layer towards the drain. In other words, this concept allows to divide, under reverse bias conditions, the maximal electric field in two parts, allowing the improvement of the breakdown voltage, for the same N^- epitaxial layer doping concentration. If the same blocking voltage as that of the conventional VDMOSFET is required, the N^- epitaxial layer doping concentration of the FLYMOSFET can be enhanced and hence the specific on-resistance will be reduced.

In the case of the conventional VDMOS device, the breakdown voltage is given by [11]:

$$V_{br} = 5.65 \times 10^{13} \times N_d^{-\frac{3}{4}}. \quad (2)$$

In the FLYMOS transistor, the breakdown voltage can be written as:

$$V_{br} = 5.65 \times 10^{13} \times N_d^{-\frac{3}{4}} + V_{ring} \quad (3)$$

where V_{ring} is the ring potential when the depletion region reaches the field ring; V_{ring} can be written as:

$$V_{ring} = \frac{q.N_d}{2.\varepsilon_s}.d^2 \quad (4)$$

where N_d and ε_s are, respectively, the doping concentration and the permittivity of the N^- epitaxial layer. q is the electron charge while d is the distance between the main junction and the floating ring.

For example, in the case of the 65 Volts VDMOSFET, the drift region doping level concentration must be equal to 7×10^{15} cm^{-3}, while it can be increased to 1.1×10^{16} cm^{-3} in the 65 Volts FLYMOSFET's case.

3 Modelling

3.1 Complete equivalent circuit

None of SPICE's standard MOSFET models fit the characteristics of vertical power MOSFETs too well. Consequently the models of MOSFET's supplied have been

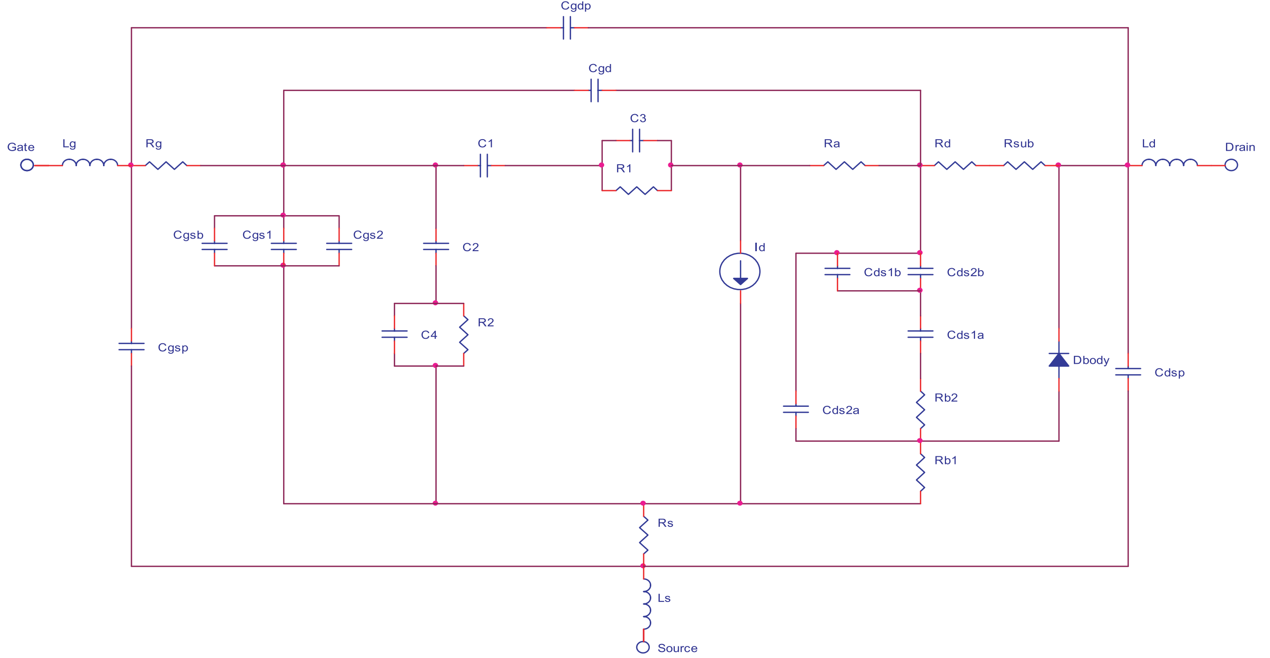

Fig. 3. Complete model of the power Vertical FLYMOSFET with one P-floating buried layer between drain and source.

made using subcircuits that include additional components to improve simulation accuracy.

The modelling approach relies on an analytical study, addressing basic equations in the semiconductor [12]. Each area of the FLYMOSFET structure — Fig. 2: (1) channel, (2) access, (3) PN junctions, (4) drift and (5) substrate — is described taking into account peculiar characteristics of the power device: short channel length (<1 μm), channel carrier mobility roll-off, current spreading in the bulk…

The equivalent circuit of the channel region consists of a current generator as well as resistive (R_1 and R_2) and capacitive (C_1 to C_4) elements (Fig. 3).

Like in the conventional VDMOSFET, the access region — i.e. intercellular region — is described in the FLYMOSFET by the gate-drain capacitance C_{gd} and the access resistance R_a. C_{gd} depends on the drain-gate voltage: it is a MOS capacitance modeled by an oxide capacitance $C_{gd\,\max}$ and a depletion capacitance C_{gddep} in series. The resistive part expressed by R_a is due to the lowly doped N^- epitaxial layer and to the pinching effect between the adjacent P diffusions.

The main difference between the FLYMOFET and the conventional VDMOSFET comes from the drain to source region: the drain to source region of the conventional structure comprises only one PN junction — this is the "P-body / N^- epitaxial layer" junction — whereas the drain to source region of the newly developed structure (FLYMOSFET) comprises two PN junctions in series — the "P-body / N^- epitaxial layer" junction and the "P-floating layer / N^- epitaxial layer" junction —. Then, this drain to source region must be represented by four junction capacitances C_{ds1a} and C_{ds1b} (corresponding to the two plane junctions) and C_{ds2a} and C_{ds2b} (corresponding to the two cylindrical junctions), two resistances R_{b1} and R_{b2} and a diode called Dbody. This diode also allows simulation of the transistor's reverse bias behavior.

Drift and substrate regions are resistive zones described by the drift resistance R_d and the substrate resistance R_{sub} respectively. Assuming that the conduction section of a FLYMOSFET is reduced by 50% compared to a conventional VDMOSFET, the optimum of R_d, depending on the breakdown voltage (V_{br}) and the number (n) of floating islands between source and drain is given by the following equation:

$$R_d(\Omega) = 16.6 \times 10^{-9} \times (V_{br})^{2.5} \times (n+1)^{-1.5} \times S^{-1} \quad (5)$$

where S is the device active area. R_{sub} is not negligible for a low voltage power MOSFET.

Capacitances C_{gs1}, due to the overlap of the gate electrode and the N^+ source, C_{gs2}, between the source and gate electrodes and C_{gsb}, between the gate electrode and the channel, series resistance R_g and parasitic elements (L_g, L_s, L_d, C_{gsp}, C_{dsp} and C_{gdp}) complete the model of the power FLYMOSFET (Fig. 3).

3.2 Reduced model

Unfortunately, this precise but stringent physical approach uses strongly nonlinear terms and results in a complex solution with a prohibitive computational time. Having to choose between model details and a reasonable numerical treatment, we decided to reduce our model, according to the 2D ATLAS simulations: the less important parameters of the model are identified and discarded, i.e. C_3, C_4, R_1, R_2, R_{b1} and R_{b2}. C_3 and C_4 are depletion capacitances in the channel: compared to other capacitances

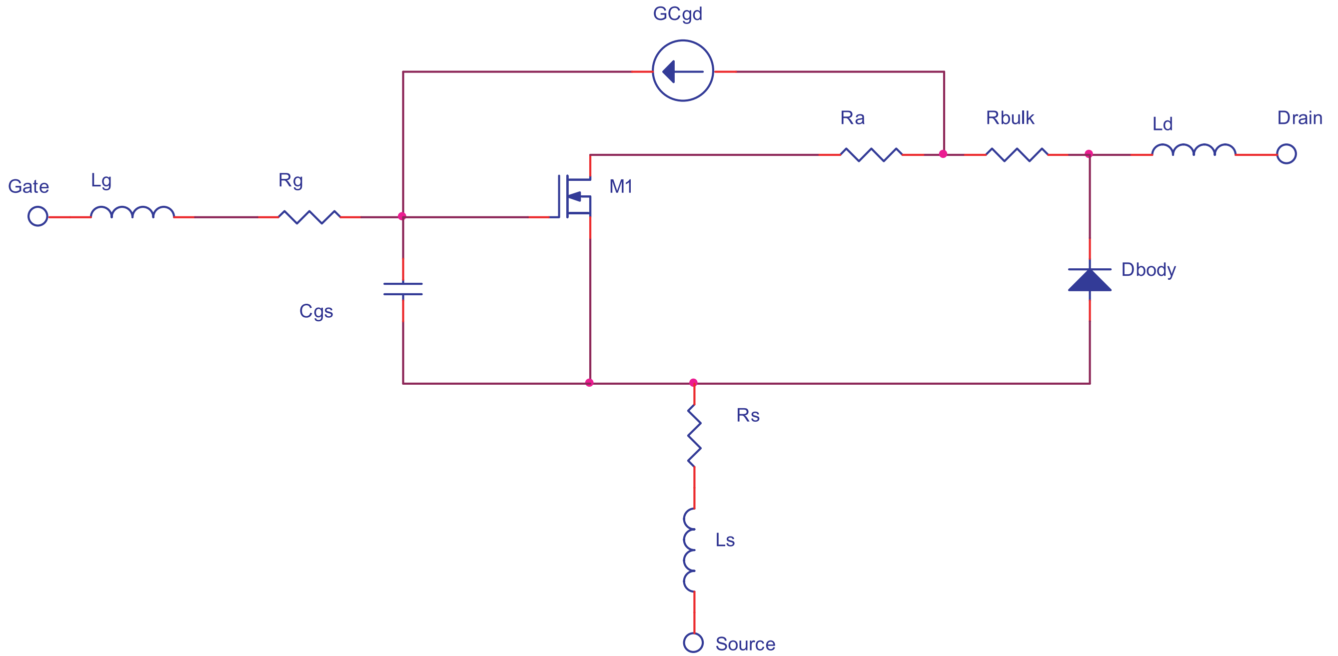

Fig. 4. Electrical reduced model of the FLYMOS transistor for switching applications.

in the circuit, they are negligible because the P-body region is highly-doped. R_1 and R_2 are also negligible compared to the channel resistance that is taken into account in the current generator I_d — see equation (6) —. Concerning R_{b1} and R_{b2}, they are also negligible resistances compared to the impedances of C_{ds1} and C_{ds2}. Parasitic elements (C_{gsp}, C_{dsp} and C_{gdp}) do not appear in the reduced model but they can be used as corrective parameters for C_{gs}, C_{ds} and C_{gd} if necessary (NB : it will not be necessary in our case).

The theoretical reduced model can be translated into SPICE circuit language, using the internal library components such as diode, MOS, capacitor, resistor, etc. Figure 4 shows the schematic diagram of the reduced sub-circuit model of the FLYMOSFET.

The role of the M1 MOSFET is explained in Section 3.2.1. The contribution of the current source G_{Cgd} is explained in Section 3.2.2. The role of the Dbody diode is explained in Sections 3.2.1 and 3.2.2.

The model's parameters were carefully identified, based on measurements and on ATLAS simulations which are sufficiently general to be applied to FLYMOS devices. Dimensions of the device are taken into account to define the parameters of the model in the following sections.

3.2.1 Static parameters

SPICE provides various MOSFET device models, which differ in the formulation of the $I_d(V_{ds})$ characteristics. The variable "LEVEL" specifies the model to be used. The "level 1" model uses very simple equations: it is not a very accurate model and it is not well adapted to power MOSFETs with short channels ($L \leqslant 1\ \mu$m). The "level 2" model uses added short channel effects, like velocity saturation, but has problems with convergence. The "level 3" model is a simplified version of "level 2", currently used for digital design. The BSIM models (levels 4, 5, 6, 7,...) use more polynomial curves fitting (less emphasis on physics than previous models): for instance, operation is divided into several regions. The SPICE "level 3" model was chosen because it combines accuracy (since it is a MOS physics-based model) and simplicity (and consequently, high simulation speed).

Then, the current generator (channel region) is described by a SPICE "level 3" MOSFET (M1 in Fig. 4). The drain currents in the triode and saturation regions are expressed respectively by the following relationships:

$$I_d = \mu_{eff} \frac{W}{L} C_{ox} \left[(V_{gs} - V_T) . V_{ds} - \alpha . \frac{V_{ds}^2}{2} \right] \quad (6)$$

$$I_d = \mu_{eff} \frac{W}{L} C_{ox} \left[(V_{gs} - V_T) . V_{sat} - \alpha . \frac{V_{sat}^2}{2} \right] \quad (7)$$

where W and L are the channel width and length respectively, C_{ox} is the gate oxide capacitance, V_{ds} is the voltage applied to the channel, V_T is the threshold voltage, V_{gs} is the gate-source voltage, V_{sat} is the drain-source voltage at the beginning of the channel pinch-off and α is a coefficient related to short and narrow channel effects. The effective carrier mobility in the inversion layer (μ_{eff}) takes into account the carrier saturation velocity in the channel ($V_{\max}$) and the reduction of mobility due to the high electric field:

$$\mu_{eff} = \frac{\mu_S}{1 + \frac{\mu_S . V_{ds}}{V_{\max} . L}} \quad \text{with:} \quad \mu_S = \frac{\mu_0}{1 + \Theta . (V_{gs} - V_T)} \quad (8)$$

where μ_S is the surface mobility in the channel inversion layer, that depends on the transverse electric field Θ — roll-off coefficient — and μ_0 the low electric field mobility.

The access resistance is represented by R_a. R_{bulk} is the series association of the drift (R_d) and substrate (R_{sub}) resistances.

The SPICE parameters are extracted and specified from measurements. At low drain voltage, the transconductance parameter K_P can be extracted from the slope factor β of the transfer characteristic $I_d(V_{gs})$.

$$\beta = \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} = K_P \cdot \frac{W}{L} \tag{9}$$

β is the gradient of the transfer characteristic $I_d(V_{gs})$ neighbouring the threshold voltage at low drain voltage ($V_{ds} = 10$ mV) in the triode region. It allows calculation of the transconductance SPICE parameter "K_P". In the saturation region, the drain saturation current is determined by the carrier saturation velocity in the channel ($V_{\max}$). Consequently, the SPICE parameter $V_{\max}$ can be obtained by adjustment of the level of the drain current in the saturation region. The SPICE parameter Θ (peculiar to SPICE "level 3" model) can be specified in the .model statement to show the dependence of the mobility on the gate electric field. The mobility modulation parameter Θ depend on the oxide thickness.

In accordance with measurements, the calculated transconductance parameter (K_P) is 380 A/V^2 (we choose to take $\beta = K_P$ with $W = L = 1$ µm in our SPICE simulation), $V_{\max}$ is specified to be equal to 1.45× 10^5 m/s and Θ is specified to be equal 0.06 V^{-1}. The threshold voltage V_T is calculated by extrapolation of the transfer characteristic $I_d(V_{gs})$ to $I_d = 0$ A: $V_T = 3.2$ V.

The Dbody diode is the representation of the "P-body / N^- epitaxial layer" junction. It takes into account the reverse bias behaviour of the FLYMOSFET. This diode can be forward-biased with negative drain voltages. In this case, the device operates as a synchronous rectifier.

3.2.2 Dynamic parameters

Values of the capacitance parameters are experimentally obtained by measuring the input ($C_{iss} = C_{gs} + C_{gd}$), output ($C_{oss} = C_{ds} + C_{gd}$) and reverse transfer ($C_{rss} = C_{gd}$) capacitances.

Recent MOSFET models mirror the performance of the real devices reasonably well in most areas. One area not covered well by the older less complex models is the way that C_{gd} and C_{ds} vary with drain-source voltage.

a) Gate-source capacitance
C_{gs} is simply represented by a constant capacitance because the gate to source capacitance is almost constant, according to our measurements and to the theory. Actually C_{gs} is the sum of three constant capacitances in parallel (C_{gs1}, C_{gs2} and C_{gsb}): they are constant because they are oxide capacitances, i.e. they only depend on the oxide thicknesses.

b) Gate-drain capacitance
The gate-drain capacitance is modeled by an oxide capacitance when $V_{dg} < 0$ and by the series association of an oxide capacitance and a depletion capacitance when $V_{dg} > 0$. Then the following expressions are used:

$$\begin{aligned} C_{gd} &= C_{gd\max} \quad \text{for} \quad V_{dg} < 0 \\ C_{gd} &= C_{gd\max} \quad \text{for} \quad V_{dg} > 0 \end{aligned} \tag{10}$$

where $C_{gd\max}$, corresponding to the gate oxide capacitance, is kept constant. The non-linear behavior of the depletion capacitance C_{gddep} is described by the following expression that is analog to the transition capacitance of the SPICE diode model:

$$C_D = \frac{C_{j0}}{\left(1 - \frac{V_a}{V_j}\right)^m} \tag{11}$$

where C_{j0} stands for zero bias capacitance ($C_{j0} = C_{gd\max}$ in the case of C_{gd}), V_a the applied voltage (i.e. V_{gd} for C_{gd}), V_j the diffusion voltage and m the ideality factor ($0 < m < 0.9$).
The gate-drain capacitance representation is made by using the controlled current source formalism (GC_{gd} — see Fig. 4 —) where the delivered current is equal to:

$$I_{dg} = \frac{C_{j0}}{\left(1 - \frac{V_a}{V_j}\right)^m} \cdot \frac{dV_{dg}}{dt} \tag{12}$$

c) Drain-source capacitance The non-linear behavior of C_{ds} as a direct function of V_{ds} is also described by equation (10) where the applied voltage (V_a) is now equal to V_{ds}. In the reduced model (Fig. 4), C_{ds} is modelled by the transition capacitance of the SPICE diode model ("Dbody" diode). This diode is very useful because, with only one device, it is possible to take into account the breakdown voltage of the device (with the "BV" parameter, which is the reverse breakdown voltage in the SPICE model of the diode) and the drain to source capacitance variations versus drain to source voltage (with the "C_{jo}", "M" and "V_j" parameters of the SPICE model of the diode).

3.2.3 Additional parameters

To complete the model, some parasitic resistive (R_g, R_s) and inductive (L_g, L_s, L_d) elements have been added. R_g is the resistance of the polysilicon gate and R_s the resistance of the source.

4 Validation of the model

The validation of the model is done by comparing SPICE simulations with measurements on an existing FLYMOSFET. This 65 Volts FLYMOSFET was fabricated with multiple parallels elementary FLYMOS cells. This method

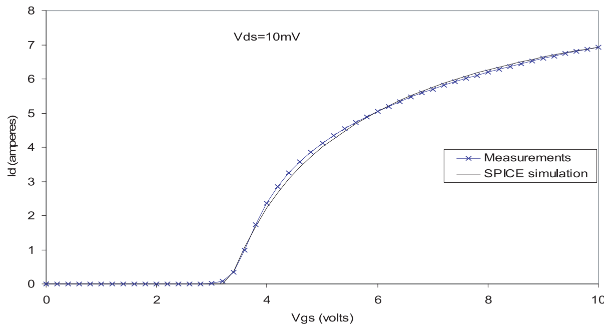

Fig. 5. Measured and SPICE simulated transfer characteristics — $I_d(V_{gs})$ — of the 65 V FLYMOSFET (V_{ds} = 10 mV).

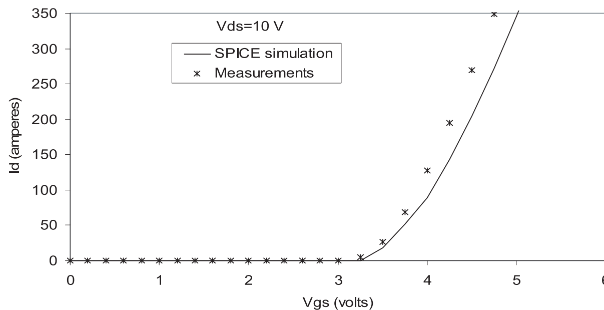

Fig. 6. Measured and SPICE simulated transfer characteristics — $I_d(V_{gs})$ — of the 65 V FLYMOSFET (V_{ds} = 10 V).

is used to increase the current in the power unipolar MOSFET transistor. The 65 Volts FLYMOSFET parameters: 1) the total area is equal to 8.41×4.56 mm^2, 2) the number of the elementary FLYMOS cells is 434×10^3, 3) the gate oxide thickness is equal to 650 Å, 4) the channel length is 0.6 μm.

4.1 Static model

Measured and SPICE simulated static characteristics — transfer $I_d(V_{gs})$ at low V_{ds} (Fig. 5) and at high V_{ds} (Fig. 6) and output $I_d(V_{ds})$ (Fig. 7) characteristics — are compared. It is obvious that a good agreement between measurements and simulated data is obtained: the difference between measured data and simulation does not exceed 19%. The difference between the simulated and measured transfer characteristics for V_{ds} = 10 Volts is due to the small reduction of the threshold voltage versus the drain voltage. Consequently, in the saturation region, drain current increases with drain voltage for the gate voltage neighbouring the threshold voltage. In the SPICE "level 3" model, the parameter taking into account this effect of short-channel on the threshold voltage is ETA (static feedback on threshold voltage). Because of the small reduction of the threshold voltage, we prefer to consider that the current saturates and its value will be constant and equal to an average value of the measured saturation currents (i.e.: ETA = 0).

The increase in the doping level of the drift region has a double effect: the reduction of the drift and access resistances. Then, in the on-state, the current level in the FLYMOSFET is higher than in the conventional VDMOSFET with the same breakdown voltage.

4.2 Drain to source capacitance

Capacitive elements have been added to the static model in order to express the stored charge of the device. Measured and SPICE simulated variations of the drain-source capacitance are presented Figure 8: a good agreement between experimental results and SPICE simulation of the FLYMOSFET is obtained. The difference between measured data and simulation does not exceed 16% (more precisely, this difference is equal to: 15.3%).

4.3 Gate to drain capacitance

In addition to the drain to source capacitance, a significant gate to drain capacitance must be included in the analysis due to the overlap of the gate electrode to the drift region. The frequency response is mainly limited by this capacitance because of the Miller effect into an equivalent input gate capacitance of the device. Figure 9 shows the measured and SPICE simulated gate to drain capacitance variations of the FLYMOSFET. As the drain bias voltage increases, C_{gd} decreases because of the depletion region developed under the oxide in the drift region. A good agreement between experimental results and SPICE simulation of the FLYMOSFET is also obtained: the difference between measured data and simulation does not exceed 17% (more precisely, this difference is equal to: 16.67%).

4.4 Gate charge measurements

To validate the model in a well-known and classical circuit used with power MOSFETs, a comparison of the measured and SPICE simulated FLYMOSFET's gate charge has also been done. Actually, switching losses are determined by the charging process of the feedback capacitance (Miller effect): low switching losses can be obtained by a low gate charge. For this test circuit (Fig. 10), the gate terminal is connected to a constant current source (2 mA), while the drain is connected to a constant voltage (10 V) supply via a current-limiting load ($R = 2\Omega$). Figure 10 shows the comparison between experimental data and SPICE simulation for the 65 Volts FLYMOSFET. A correct agreement is also obtained. The main difference between simulation and measurements is due to the fact that the gate to source capacitance $C_{gs}(C_{gs} = C_{gsb} + C_{gs1} + C_{gs2})$ is kept constant in our reduced model. In fact, for $V_{gs} > V_T$, the device is turned on and the gate to source capacitance is dependent on V_{ds} [13].

5 Conclusion

In this paper, a complete SPICE-compatible subcircuit model has been proposed for the first time to

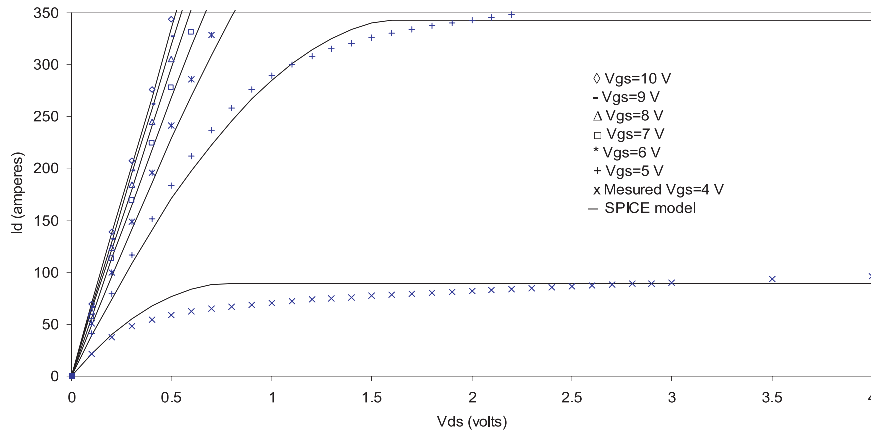

Fig. 7. Measured and SPICE simulated output characteristics — $I_d(V_{ds})$ — of the 65 V FLYMOSFET.

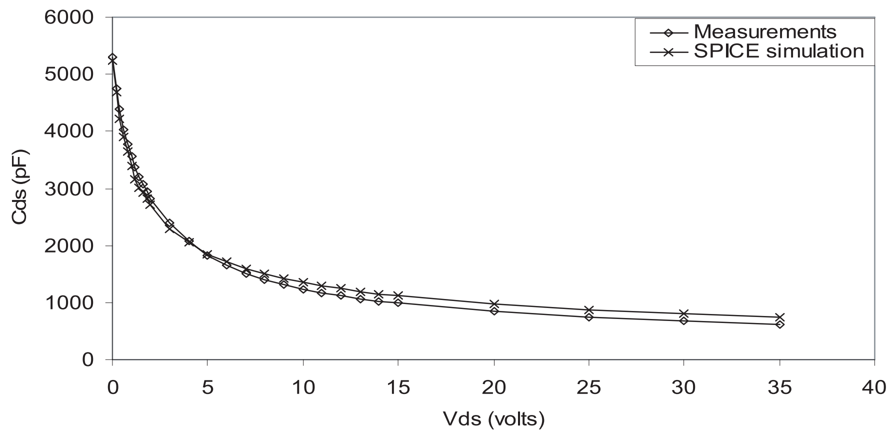

Fig. 8. Measured and SPICE simulated drain to source capacitance C_{ds} variations versus V_{ds} of the 65 V FLYMOSFET.

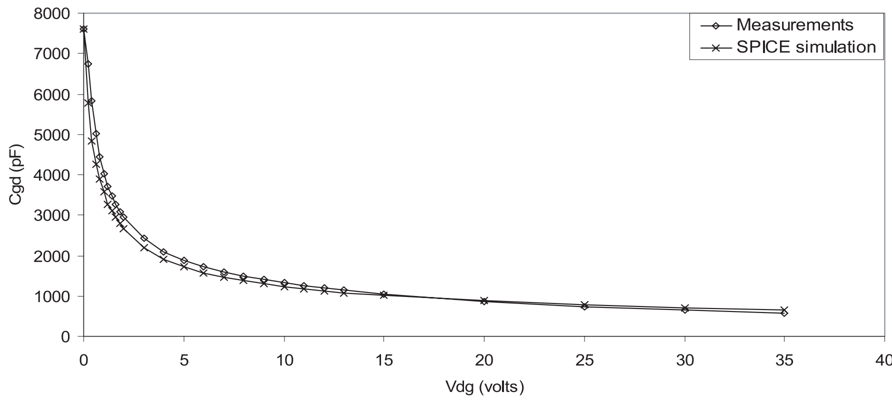

Fig. 9. Measured and SPICE simulated gate to drain capacitance C_{gd} variations versus V_{dg} of the 65 V FLYMOS.

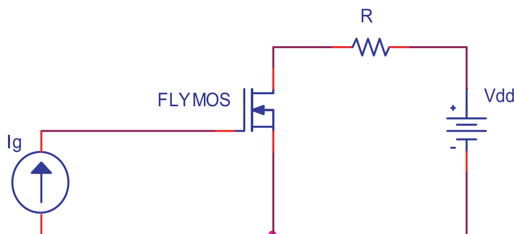

Fig. 10. Schematic diagram of the circuit used in the gate charge measurement with $R = 2\ \Omega$, $I_g = 2$ mA and $V_{dd} = 10$ Volts.

simulate static and dynamic behaviour of the recently developed power FLYMOSFET. Unfortunately, this precise but stringent physical approach used strongly nonlinear terms and results in a complex solution with a prohibitive computational time. Having to choose between model details and a reasonable numerical treatment, we first decided to reduce our model. Then measured and SPICE-simulated (with the reduced model) static and dynamic characteristics have been compared and have shown the reliability of our approach: a good agreement has been obtained between experimental results and simulations.

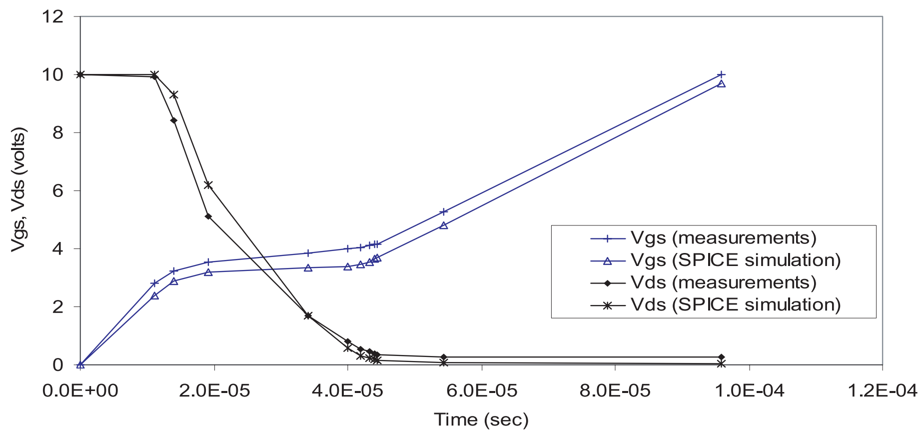

Fig. 11. Measured and SPICE simulated gate charge waveforms of the 65 Volts FLYMOSFET.

Furthermore, these simulations are very fast. Then, this model will be suited in switching power electronics applications.

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