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A general modelling and control algorithm of a three-phase multilevel diode clamped inverter by means of a direct space vector control

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Abstract. This paper presents a simple and general direct modulation strategy that enables to copy directly modulated waveforms onto output voltages of a multilevel three-phase Diode Clamped Inverter (DCI). A general modelling of this converter is presented. A space vector scheme is developed without using Park transforms. Based on this algorithm, the location of the reference voltage vector is determined and the voltage vectors for the modulation are deduced. Simultaneously, their durations are calculated. The proposed algorithm is general and can be directly applied to a $(n+1)$ levels inverter independently on its topology (Diode Clamped Inverter, Neutral Point Clamped, Flying Capacitor Inverter...). To verify this algorithm, both control algorithms of a 5-level DCI and a 11-level DCI are considered and simulation results are given.

PACS. 84.30.jc Power electronics; power supply circuits – 84.30.bv Circuit theory (including computer-aided circuit design and analysis)

1 Introduction

Voltage source multilevel inverters are more and more used in many industrial applications such as AC power supplies, static VAR compensators, etc. One of the significant advantages of multilevel converters is the harmonic reduction in the output waveform without increasing the switching frequency and without decreasing the inverter power output. The output voltage waveform of a voltage source multilevel inverter is composed of intermediary voltage levels, which are obtained from capacitor voltage sources [1–4].

In the past, many algorithms have been developed to control the two-level inverter, as, triangulo-sinusoidal, hysteresis control, Space Vector Modulation... But these algorithms can not be directly generalized to $(n+1)$ levels inverter. In the last decade, extensions of these algorithms to multi-level inverters have been proposed and developed in many contexts [5–9]. Recently, a direct modulation strategy has been developed for a single phase three-level Neutral Point Clamped (NPC) [4]. It has been extended to a three-phase three-level NPC in [10] and also to a single-phase five-level inverter in [11]. Moreover, the general direct modulation has been developed to a single-phase multilevel inverter in [12]. New general space vector PWM control algorithms for multilevel inverters [13,14] have been developed last years. In these algorithms, the use of the space vector diagram increases calculations. In the direct modulation [10], the vector modulation generates line-to-line voltages without using a Park transform. So, the calculations are very simple. For this reason, these modulation algorithms are investigated for $(n+1)$-level inverters and a new general direct modulation is proposed.

In this paper, the principle of a general modulation strategy without Park transformation (in a d, q frame) is developed. Firstly, the particular multilevel inverter operating principle and the modelling of this converter are presented. This appropriate average modelling is used for the control design. Therefore, a new vector control scheme is presented. As usually, the frame is divided into triangular areas. The three vectors related with the area that includes the reference vector are used to create the PWM

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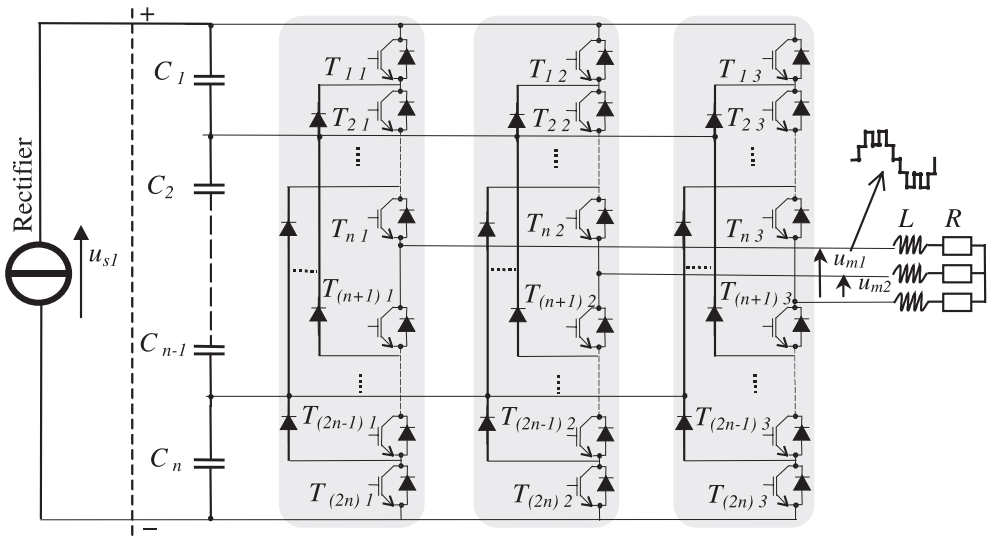


Fig. 1. Schematic diagram of the three-phase (n+1) levels converter.

waveform [10,15]. The space frame is not obtained through a mathematical transformation but is directly the line-to-line voltage space. ($3n^2$+$3n$+1) voltage vectors are used for the modulation. The mathematical development is detailed and the simple implementation of this modulator is given. The presented simulation results show the very good performances obtained with this modulation technique for a five-level and an eleven-level Diode Clamped Inverters (DCI).

2 General modelling of the three phase (n + 1) level DCI

2.1 Structure and operating principle

The topology of the $(n+1)$ levels DCI consists of three commutation circuits, which are fed with a capacitive divider (Fig. 1). The three commutation circuits of $2\times n$ transistors enable to make reversible the modulated voltages um_1 and um_2. As the load current is alternative, the required switches are made of $2\times n$ transistors with anti-parallel diodes. Additional steering diodes are required to clamp one terminal of each transistor to the shared capacitor points.

As switches are switch-on and switch-off controlled, their states and external gate signals are dependent. Therefore, the converter can operate in PWM mode to shape the modulated voltage in a multilevel waveform. The modulation frequency must be chosen higher than the highest required load frequency and smaller than the maximum transistor switching frequency.

2.2 Fundamental principles of DCI

The diode clamped multilevel inverter uses capacitors in series to divide the DC bus voltage into a set of intermediary voltage levels. To produce (n+1) voltage levels, an n-level diode-clamped inverter needs n capacitors i.e. C_1, C_2, C_3, ..., and C_n which are connected to a DC bus voltage source us_1. The voltage across each capacitor is $\frac{us_1}{n}$.

Looking at the first clamped commutation circuit (Fig. 2a), the output voltage (v_{c0}) may be equal to:

- the full level (us_1) by switching on the sets $\{T_{1c}, D_{1c}\}, \{T_{2c}, D_{2c}\}$, ... and $\{T_{nc}, D_{nc}\}$,
- the $\frac{(n-1)}{n}.us_1$ level by switching on the sets $\{T_{2c}, D_{2c}\}, \{T_{3c}, D_{3c}\}, \ldots$ and $\{T_{(n+1)c}, D_{(n+1)c}\}$,
- ...,
- the zero level by switching on the sets $\{T_{(n+1)c}, D_{(n+1)c}\}, \{T_{(n+2)c}, D_{(n+2)c}\}, \ldots$ and $\{T_{(2n)c}, D_{(2n)c}\}$.

Therefore, this clamped commutation circuit is equivalent to a commutation circuit (Fig. 2b) where one ideal switch f_{rc} among $(n+1)$ switches is at anytime switched on. The switch states are called switching functions (f_{rc}). If $f_{rc} = 1$, the corresponding ideal switch (and so corresponding transistors-diodes) is closed. Otherwise, if $f_{rc} = 0$, it is open. r is the number of the ideal matrix row and c is the colon, $r \in \{1, \ldots, n, n+1\}, c \in \{1, 2, 3\}$. The last switching function is deduced from the other ones as: $f_{(n+1)c} = \bar{f}_{1c} \times \bar{f}_{2c} \times \cdots \times \bar{f}_{nc}$.
(n+1) configurations of each commutation circuit (c) exist and connect three phases from the capacitor voltage divider to the load (Tab. 1). Hence by considering a continuous conduction mode, an equivalent converter with ideal switches may be considered for an easier study (Fig. 3).
Therefore, switching functions (f_{rc}) are defined as (Tab. 1):

$$f_{rc} = T_{rc}T_{(r+1)c} \cdots T_{(r+n-1)c}, \text{ for } r \in \{1, \ldots, n\}. \quad (1)$$

In order to implement wished switching functions (f_{ref-rc}), corresponding gate signals of transistors are

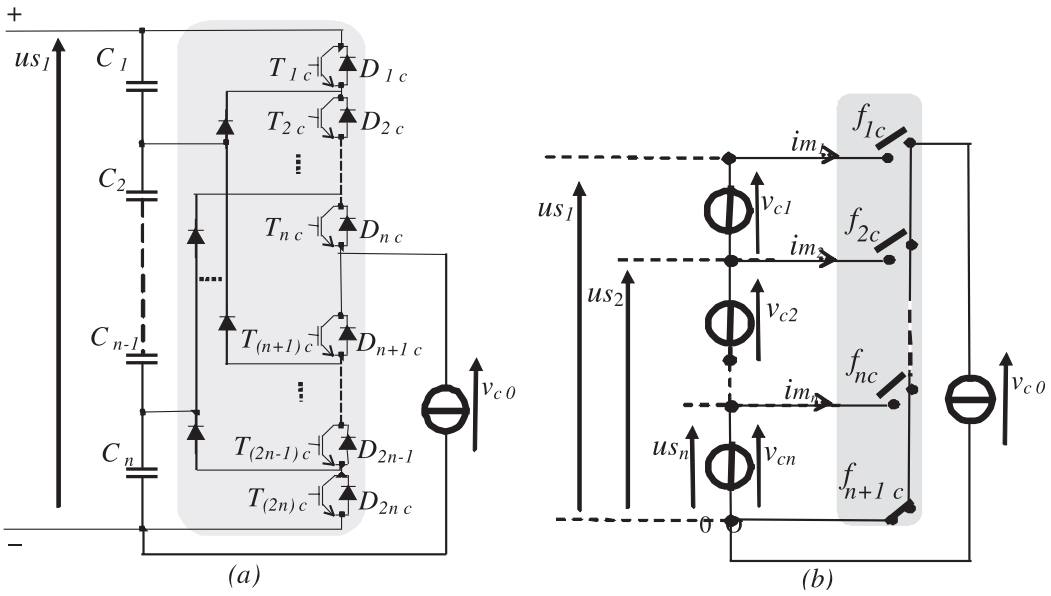


Fig. 2. Equivalent commutation circuit, $c \in \{1, 2, 3\}$.

Table 1. Equivalent commutation circuit.

Gate signals										Switching functions					v_{c0}
T_{1c}	T_{2c}	...	$T_{(n-1)c}$	T_{nc}	$T_{(n+1)c}$	$T_{(n+2)c}$	...	$T_{(2n-1)c}$	$T_{(2n)c}$	f_{1c}	f_{2c}	...	f_{nc}	$f_{(n+1)c}$	
1	1	...	1	1	0	0	...	0	0	1	0	...	0	0	us_1
0	1	...	1	1	1	0	...	0	0	0	1	...	0	0	$\frac{(n-1)}{n}.us_1$
		:					:					:			:
0	0	...	1	1	1	1	...	0	0	0	0	...	0	0	$\frac{2}{n}.us_1$
0	0	...	0	1	1	1	...	1	0	0	0	...	1	0	$\frac{1}{n}.us_1$
0	0	...	0	0	1	1	...	1	1	0	0	...	0	1	0

set by:

$$\begin{cases} T_{1c} = f_{ref-1c} \\ T_{2c} = f_{ref-1c} + f_{ref-2c} \\ \vdots \\ T_{nc} = f_{ref-1c} + f_{ref-2c} + \cdots + f_{ref-nc}. \end{cases} \quad (2)$$

A general expression can be used as:

$$T_{rc} = \sum_{j=1}^{r} f_{ref-jc}$$

for $r \in \{1, \ldots, n\}$, $c \in \{1, 2, 3\}$ and $T_{(n+r)c} = \bar{T}_{rc}$.

2.3 Connection operating modelling

For an easier analysis of the discontinuous operation and to establish the mathematical description of the voltage conversion, we use the representation which is depicted in Figure 3. This one is obtained from Figure 1:

– by replacing all reactive elements (which are connected to switches) by their equivalent electrical sources (a self by a current source and a capacitor by a voltage source),

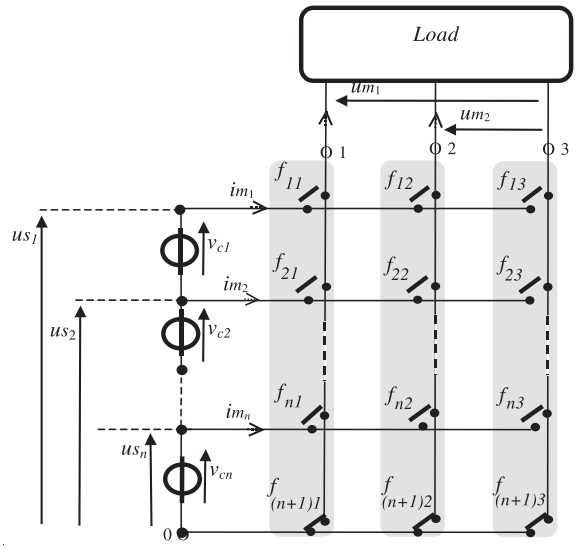


Fig. 3. Equivalent matrix structure of a multilevel converter with three commutation cells of $(n+1)$ switches.

– by considering only two phase to phase modulated voltages (the third one is linked to others). We will show that this non-trivial choice will simplify greatly the design of the control algorithm,

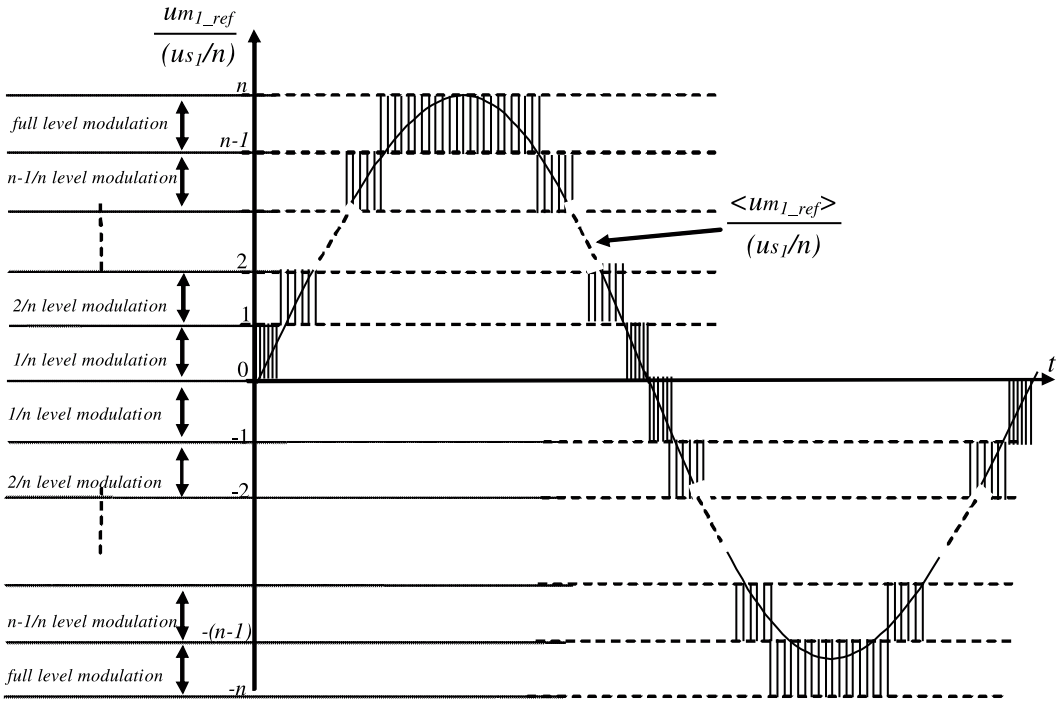


Fig. 4. Modulation operation regions and corresponding modulated voltage.

– by gathering all ideal switches in a matrix containing vertical equivalent commutation circuits as explained in the previous section [10].

Phase to neutral (point 0) modulated voltages are mathematically expressed by the following equations (Fig. 2):

$$v_{c0} = \Big(v_c - v_0\Big) = \sum_{r=1}^{n} f_{rc}.us_r \tag{3}$$

and phase-to-phase modulated voltages are expressed by:

$$um_1 = v_{10} - v_{30} = \sum_{r=1}^{n}(f_{r1} - f_{r3}).us_r \tag{4}$$

$$um_2 = v_{20} - v_{30} = \sum_{r=1}^{n}(f_{r2} - f_{r3}).us_r. \tag{5}$$

2.4 Conversion modelling

As input voltage sources are supposed to have constant values, it appears that each phase-to-phase modulated voltage is shaped through n elementary modulated voltages as:

$$um_1 = \sum_{r=1}^{n} vm_{r1}, \text{ and } um_2 = \sum_{r=1}^{n} vm_{r2} \tag{6}$$

or,

$$um_p = \sum_{r=1}^{n} vm_{rp} \text{ with } p \in \{1, 2\}. \tag{7}$$

The elementary modulated voltages are expressed as:

$$vm_{rp} = m_{rp}.\, us_r \text{ , with } r \in \{1, \ldots, n\} \text{ and } p \in \{1, 2\} \tag{8}$$

with

$$m_{rp} = f_{rp} - f_{r3}. \tag{9}$$

2.5 Analysis of multilevel operating

The multilevel voltage is a consequence of the combination of n DC capacitor voltages (us_n). A simultaneous magnitude and width modulation is possible. By using levels 0 and $\frac{u_{s1}}{n}$, we get a $\frac{1}{n}$ level modulation. By using levels $\frac{1}{n}.u_{s1}$ and $\frac{2}{n}.u_{s1}$, we obtain a $\frac{2}{n}$ level modulation and so one. By using $\frac{(n-1)}{n}.u_{s1}$ and u_{s1}, we obtain a full level modulation, as depicted for the case of a sinusoidal voltage reference $\frac{\langle um_{1-ref}\rangle}{us_1/n}$ in Figure 4 [10,12].

2.6 Average modelling

The purpose of the control system is to regulate the equivalent mean value of modulated voltages inside each modulation period [4]. The mean value of a modulated voltage during the modulation period (T_m) is expressed as:

$$\Big\langle um_p(t)\Big\rangle = \left[\frac{1}{Tm}.\int_{k.Tm}^{(k+1).Tm} um_p(t)dt\right], \quad \text{with } k \in N \text{ and } t \in [k.Tm,\, (k+1).Tm]. \tag{10}$$

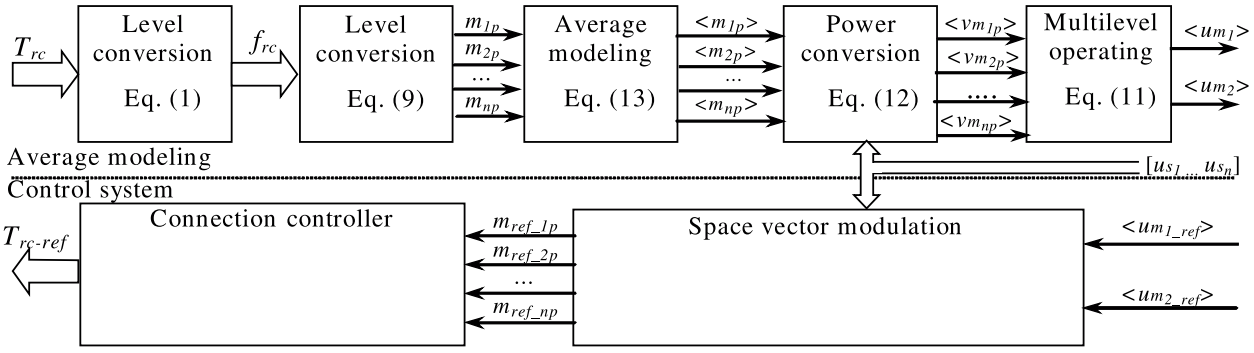


Fig. 5. Control architecture of the multilevel inverter.

This quantity is linked to modulation functions and voltage sources (Eqs. (7–9)), which are assumed to be nearly constant during the modulation period:

$$\left\langle um_p(t)\right\rangle = \sum_{r=1}^{n} \left\langle vm_{rp}(t)\right\rangle \tag{11}$$

with

$$\langle vm_{rp}(t)\rangle = \langle m_{rp}(t)\rangle .us_r. \tag{12}$$

The mean value of a modulation function is therefore defined as:

$$\left\langle m_{rp}(t)\right\rangle = \left[\frac{1}{Tm}.\int_{k.Tm}^{(k+1).Tm} m_{rp}(t).dt\right]. \tag{13}$$

This value corresponds to a signed voltage ratio, which is defined according to one capacitor voltage (us_n).

3 Design of the control system

3.1 General control scheme

All presented equations of the modelling part are used to describe control actions. The ordering of all implicated relations following the input output transfer and the causality respect gives the representation, which is depicted in Figure 5 [10,12].

In order to ensure a correct multilevel operating, the control system is built around a connection controller and a space vector modulator. The connection controller processes corresponding gate signals in order to set a wished modulation functions via equation (2) and the inverse of equation (9). The space vector modulator is now detailed.

3.2 Space vector modulation for multilevel operation

The $(3n^2 + 3n + 1)$ different configurations for the voltage space vector are represented in the frame $\left(0, \frac{\vec{u}m_1}{us_1/n}, \frac{\vec{u}m_2}{us_1/n}\right)$(Fig. 6). Each location of the space vector is described by indexes as i and j, $\vec{u}(i,j)$ with $(i,j) \in \{(-n,-n),...,(n,n)\}$: We join two different vectors by a line if there is a way to join them by commutation in only one commutation circuit. The frame is consequently divided into $(2{\cdot}3{\cdot}n^2)$ triangular areas. The average value of both modulated voltages may be set by switching respectively the three vectors, which define the sector where the wished voltage vector is located. The proposed vectorial approach has been already used for a five-phase two-level inverter [6] and for a three–phase three–level inverter [10]. This technique enables to compute explicitly the durations. An analytical development is used to have simple and general algebra equations for optimization. The duration of each vector is determined by obtained projections onto the frame vectors ($\left(0, \frac{\vec{u}m_1}{us_1/n}, \frac{\vec{u}m_2}{us_1/n}\right)$). For all square areas four triangular sectors have to be considered (Fig. 7). To obtain a simple and general algorithm, we use the sectors ① and ②. The two sectors ③ and ④ may be also employed if one wants to make the DC link balancing using these redundant vectors or to minimize the number of commutations.

The function ($y = sign(x)$) is defined as:

$$y = 1 \text{ if } x > 0 \tag{14}$$

$$y = -1 \text{ if } x < 0. \tag{15}$$

Elementary duty cycles of modulated voltages according to the smallest level ($\frac{us_1}{n}$) are defined as:

$$r_1 = \frac{\langle um_1\rangle}{us_1/n}, r_2 = \frac{\langle um_2\rangle}{us_1/n} \tag{16}$$

where $\langle um_1\rangle$ and $\langle um_2\rangle$ are the mean values of corresponding modulated voltages.

The sector where the vector is located may be detected by using a quantification function (fix) which is defined as (Fig. 8):

$$y = fix(x) = a \text{ if } x \in [a,\ a + sign(a)[, \text{with } a \in Z. \tag{17}$$

This sector is found thanks to parameters i and j:

$$i = fix(r_1),\ j = fix(r_2) \tag{18}$$

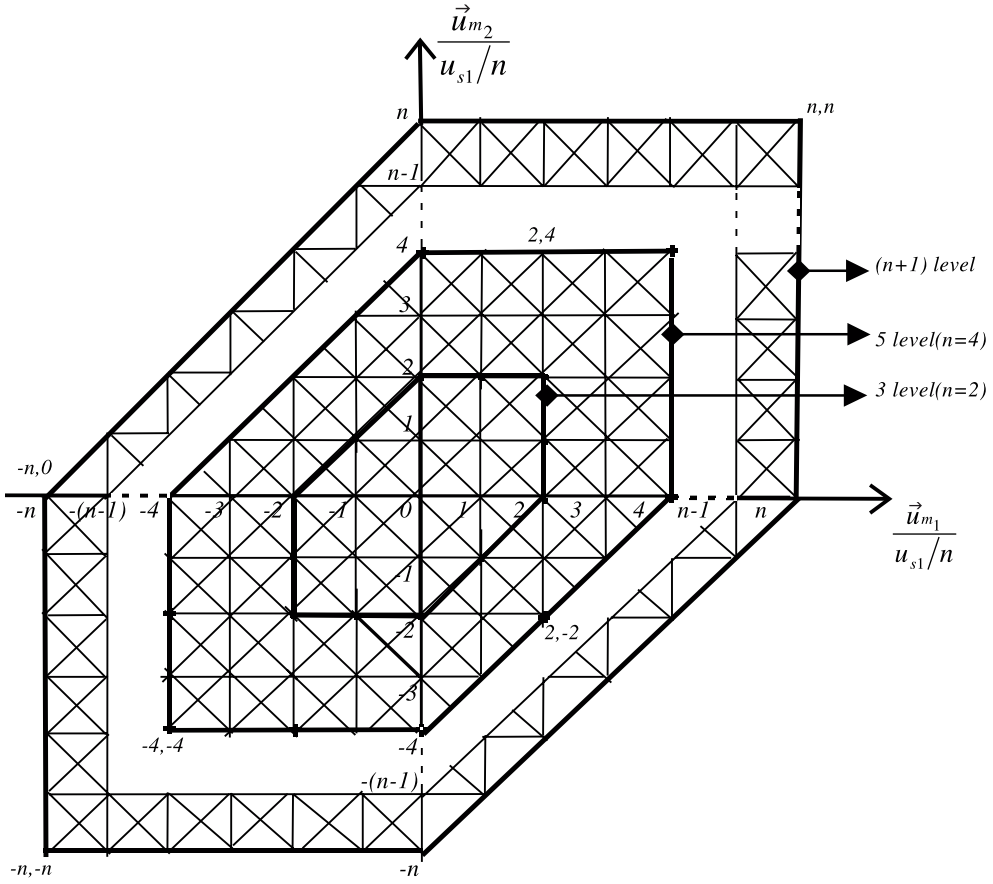


Fig. 6. Space vector location into the frame $\left(0, \frac{\vec{u}m_1}{us_1/n}, \frac{\vec{u}m_2}{us_1/n}\right)$.

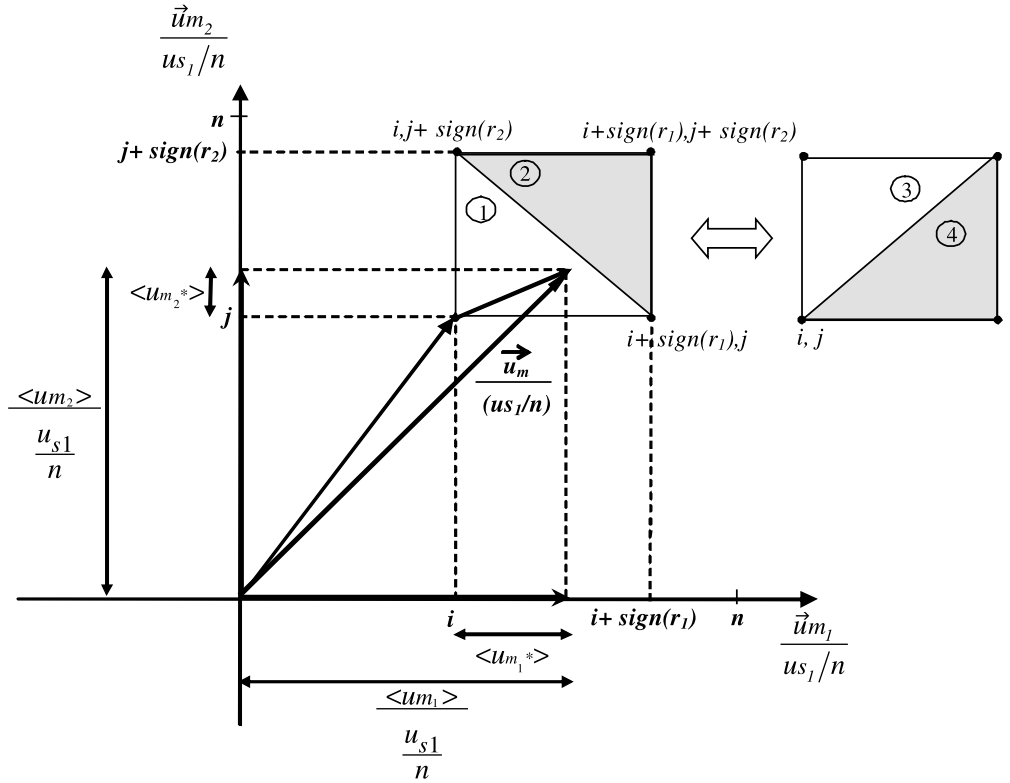


Fig. 7. Expanded view of the studied sector.

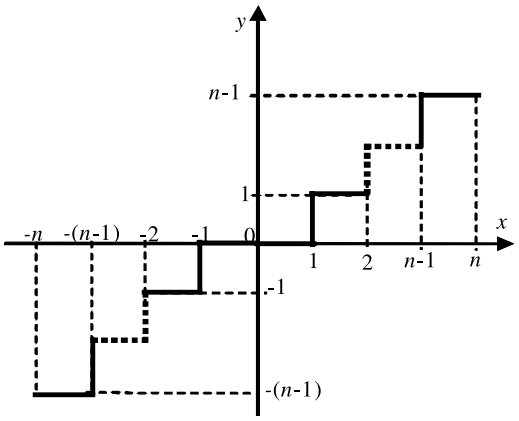


Fig. 8. Graphical representation of the function *fix*.

If the wished voltage vector is located as depicted in Figure 7, two sectors which are defined by three vectors can be considered:
Sector ①:

$$\vec{u}_1 = u(i,\, j),\ \vec{u}_2 = \vec{u}\,(i + sign\,(r_1), j) \text{ and } \vec{u}_3 = \vec{u}(i,\, j + sign\,(r_2)) \quad (19)$$

or
Sector ②:

$$\vec{u}_1 = u(i + sign(r_1),\, j + sign(r_2)), \vec{u}_2 = \vec{u}(i, j + sign(r_2)) \text{ and } \vec{u}_3 = \vec{u}(i + sign(r_1), j). \quad (20)$$

The modulated voltage vector can be timely generated by applying vectors $\vec{u}_1$, $\vec{u}_2$ and $\vec{u}_3$ during respective durations t_1, t_2, t_3 (Fig. 9):

$$\frac{\vec{u}m}{u_{s1}/n} = \frac{t_1}{T_m}.\vec{u}_1 + \frac{t_2}{T_m}.\vec{u}_2 + \frac{t_3}{T_m}.\vec{u}_3 \quad (21)$$

with the following variation domains $\frac{\vec{u}m}{us_1/n}, \vec{u}_1, \vec{u}_2\, and\, \vec{u}_3 \in \{(-n,-n), \ldots, (n,n)\}$.
In fact only two durations must be determined because all durations must be equal to the modulation period T_m:

$$t_1 + t_2 + t_3 = T_m. \quad (22)$$

Let us consider that the duration (t_1) of vector $\vec{u}_1$ is fixed by the previous equation witch yields to $t_1 = T_m - t_2 - t_3$ then using equation (21) and this equation, we obtain:

$$\frac{\vec{u}m}{u_{s1}/n} = \frac{1}{T_m}.\,(t_2.\,(\vec{u}_2 - \vec{u}_1) + t_3.(\vec{u}_3 - \vec{u}_1) + T_m.\vec{u}_1). \quad (23)$$

If we consider the projections of the reference voltage vector onto axis $\left(0, \frac{\vec{u}m_1}{us_1/n}, \frac{\vec{u}m_2}{us_1/n}\right)$ the considered modulated voltage can be also expressed as:

$$\frac{\vec{u}m}{u_{s1}/n} = \frac{\langle u_{m1}\rangle}{u_{s1}/n}.\frac{\vec{u}_{m1}}{u_{s1}/n} + \frac{\langle u_{m2}\rangle}{u_{s1}/n}.\frac{\vec{u}_{m2}}{u_{s1}/n}. \quad (24)$$

Another expression can be obtained by using the location of the operation domain (i, j) and per unit durations of modulated voltages $(\langle um_1^*\rangle, \langle um_2^*\rangle)$ which corresponds to this domain as (Fig. 7):

$$\frac{\vec{u}m}{u_{s1}/n} = (i + \langle um_1^*\rangle).\frac{\vec{u}m_1}{u_{s1}/n} + (j + \langle um_2^*\rangle).\frac{\vec{u}m_2}{u_{s1}/n}. \quad (25)$$

In each triangular area, we can define per unit durations of modulated voltages by:

$$\langle um_1^*\rangle = r_1 - i$$

$$\langle um_2^*\rangle = r_2 - j.$$

1. If the modulation voltage is located in triangle ①, i.e. $|\langle um_1^*\rangle| + |\langle um_2^*\rangle| \leq 1$, the vector $\vec{u}_1 = \vec{u}(i,j)$ is chosen as the corner vector. Then the modulated voltage vector is expressed with this vector as:

$$\vec{u}_1 = \vec{u}(i,j) = i.\frac{\vec{u}m_1}{us_1/n} + j.\frac{\vec{u}m_2}{us_1/n}. \quad (26)$$

Subtractions of vectors from the triplet are unity as:

$$\vec{u}_2 - \vec{u}_1 = sign(r_1)\frac{\vec{u}m_1}{us_1/n} \quad (27)$$

$$\vec{u}_3 - \vec{u}_1 = sign(r_2)\frac{\vec{u}m_2}{us_1/n}. \quad (28)$$

Equation (23) becomes:

$$\frac{\vec{u}m}{us_1/n} = \frac{1}{T_m}\left(t_2 sign(r_1)\frac{\vec{u}m_1}{us_1/n} + t_3 sign(r_2)\frac{\vec{u}m_2}{us_1/n} + T_m\left(i.\frac{\vec{u}m_1}{us_1/n} + j.\frac{\vec{u}m_2}{us_1/n}\right)\right) \quad (29)$$

$$\frac{\vec{u}m}{us_1/n} = \left(\left(\frac{t_2}{T_m}sign(r_1) + i\right)\frac{\vec{u}m_1}{us_1/n} + \left(\frac{t_3}{T_m}sign(r_2) + j\right)\frac{\vec{u}m_2}{us_1/n}\right). \quad (30)$$

By equaling equations (25, 30), we deduce time durations of vectors:

$$t_2 = Tm.\langle um_1^*\rangle.sign(r_1), \text{ and } t_3 = Tm.\langle um_2^*\rangle.sign(r_2). \quad (31)$$

These durations can be expressed as:

$$t_2 = Tm.|\langle um_1^*\rangle|, \text{and } t_3 = Tm.|\langle um_2^*\rangle|. \quad (32)$$

2. If the modulation voltage is located in triangle ②, i.e. $|\langle um_1^*\rangle| + |\langle um_2^*\rangle| > 1$, the vector $\vec{u}_1 = \vec{u}(i + sign(r_1), j + sign(r_2))$ is chosen as the corner vector. Then the modulated voltage vector is expressed with this vector as:

$$\frac{\vec{u}m}{us_1/n} = \vec{u}(i + sign(r_1), j + sign(r_2)) + (\langle um_1^*\rangle - sign(r_1)) \times \frac{\vec{u}m_1}{us_1/n} + (\langle um_2^*\rangle - sign(r_2))\frac{\vec{u}m_2}{us_1/n} \quad (33)$$

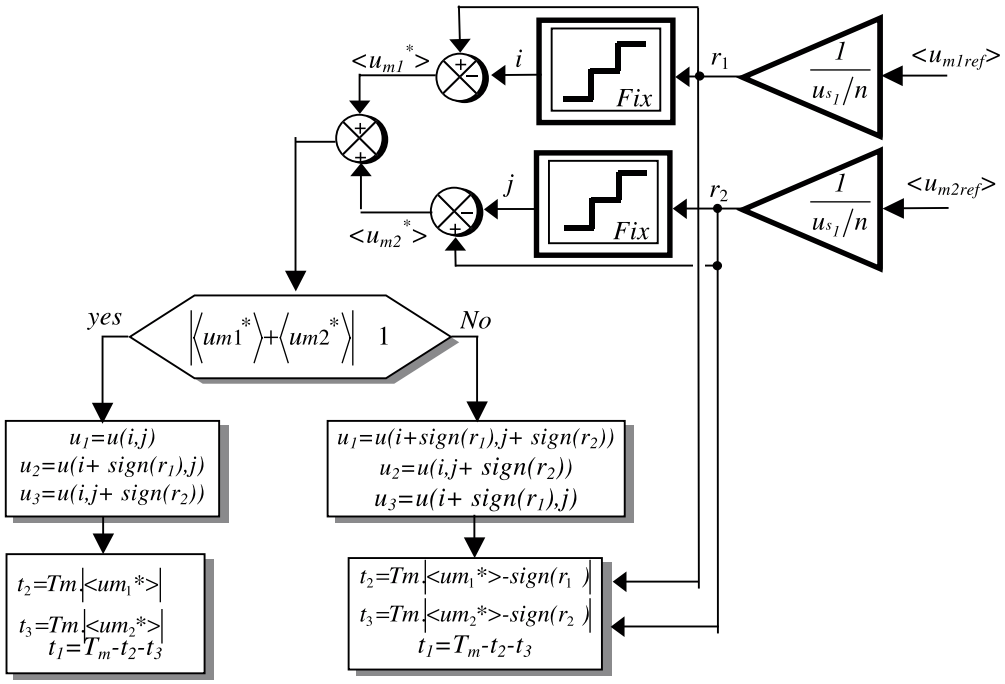


Fig. 9. Implementation of the conversion controller.

with

$$\vec{u}(i+sign(r_1),j+sign(r_2)) = (i+sign(r_1))\frac{\vec{u}m_1}{us_1/n} + (j+sign(r_2))\frac{\vec{u}m_2}{us_1/n}. \quad (34)$$

We obtain:

$$\frac{\vec{u}m}{us_1/n} = \left(i+\left\langle um_1^{*}\right\rangle\right)\frac{\vec{u}m_1}{us_1/n} + \left(j+\left\langle um_2^{*}\right\rangle\right)\frac{\vec{u}m_2}{us_1/n}. \quad (35)$$

Now we considering the following triplet of vectors:

$$\begin{aligned}&\vec{u}_1 = u(i+sign(r_1),j+sign(r_2)),\\ &u_2 = \vec{u}(i,j+sign(r_2)) \text{ and}\\ &\vec{u}_3 = (i+sign(r_1),j).\end{aligned} \quad (36)$$

Then we get following expressions:

$$\vec{u}_2-\vec{u}_1 = -sign(r_1)\frac{\vec{u}m_1}{us_1/n} \quad (37)$$

$$\vec{u}_3-\vec{u}_1 = -sign(r_2)\frac{\vec{u}m_2}{us_1/n} \quad (38)$$

$$\begin{aligned}\vec{u}_1 =& \vec{u}\,(i+sign(r_1),\, j+sign(r_2))\\ =& (i+sign(r_1))\,\frac{\vec{u}m_1}{us_1/n}\\ &+ (j+sign(r_2))\,\frac{\vec{u}m_2}{us_1/n}.\end{aligned} \quad (39)$$

Equation (23) is rewritten as:

$$\frac{\vec{u}m}{us_1/n} = \left(\left(-\frac{t_2}{T_m}sign(r_1)+i+sign(r_1)\right)\frac{\vec{u}m_1}{us_1/n} + \left(-\frac{t_3}{T_m}sign(r_2)+j+sign(r_2)\right)\frac{\vec{u}m_2}{us_1/n}. \quad (40)$$

After identification of this vector with coordinates of the wished modulation vector equation (35), durations are easily found:

$$t_2 = T_m\left|\left\langle um_1^{*}\right\rangle - sign(r_1)\right|, \text{ and}$$
$$t_3 = T_m\left|\left\langle um_2^{*}\right\rangle - sign(r_2)\right|. \quad (41)$$

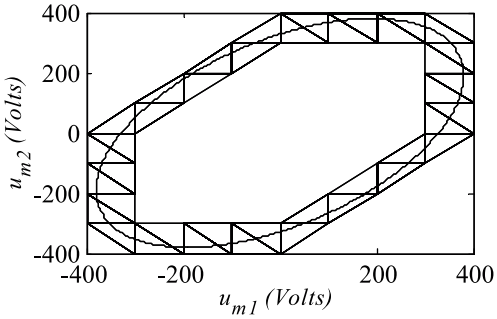
4 Simulation results

Using the developed general modelling and control algorithm, the voltage waveforms of a five-level DCI and an eleven-level DCI are shown in Figures 10 and 11. The fundamental frequency is 50 Hz and the modulation frequency is 5 kHz.

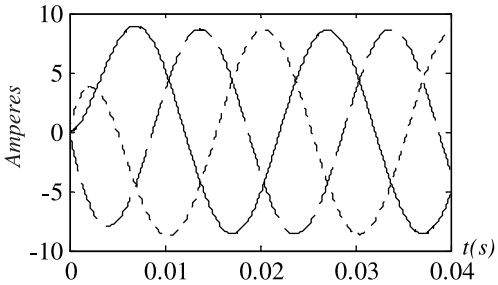
The reference line to line voltage draws an ellipse in the frame $\left(0, \frac{\vec{u}m_1}{us_1/n}, \frac{\vec{u}m_2}{us_1/n}\right)$, corresponding used sectors are shown (Figs. 10a, 11a).

Figures 10b and 11b shows the three-phase output line currents of the inverter which have good sinusoidal waveforms.

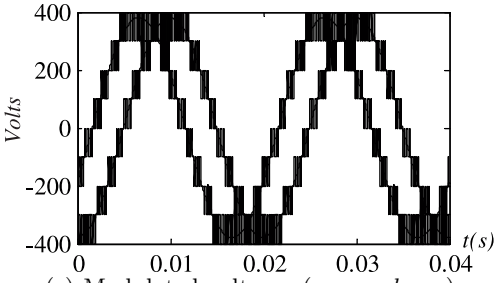
The line to line modulated voltages and their references are depicted in Figures 10c and 11c. The obtained line



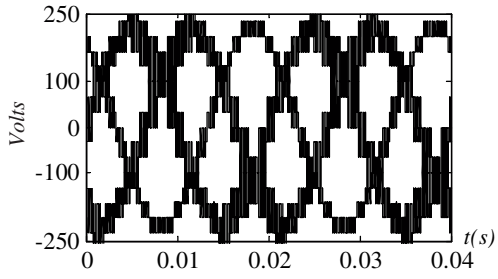
(a) Reference modulated voltages and used vectors



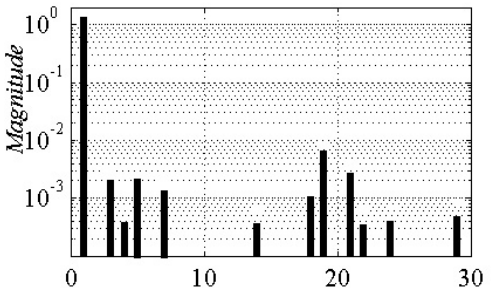
(b) Load currents



(c) Modulated voltages (u_{m1} *and* u_{m2})

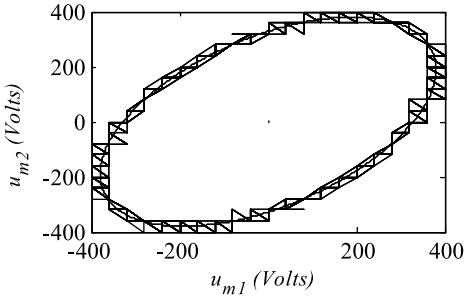


(d) Modulated voltages (v_{10}, v_{20} *and* v_{30})

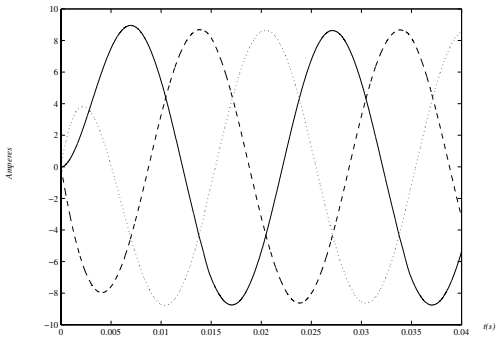


(e) Harmonic spectrum of the modulated voltage v_{10}

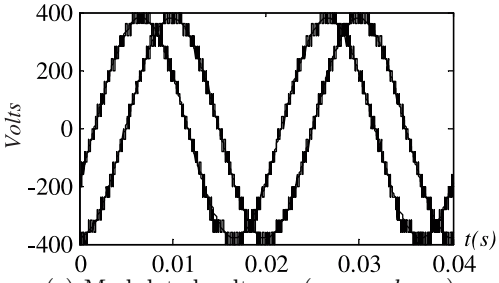
Fig. 10. Simulation results with a 5-level inverter.



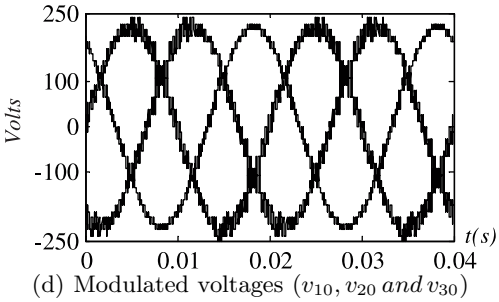
(a) Reference modulated voltages and used vectors



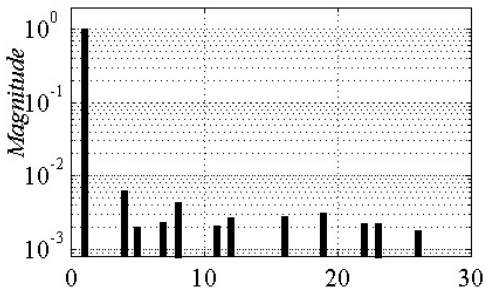
(b) Load currents



(c) Modulated voltages (u_{m1} *and* u_{m2})



(d) Modulated voltages (v_{10}, v_{20} *and* v_{30})



(e) Harmonic spectrum of the modulated voltage v_{10}

Fig. 11. Simulation results with a 11-level inverter.

voltages are shown in Figures 10d and 11d. The FFT (harmonic spectrum) of the first line voltage v_{10} is calculated and depicted in Figures 10e and 11e. In front of the fundamental component, one notes that higher harmonics are negligible and their maximum value is approximately 0.85% for the five-level and 0.6% for eleven-level. Since, in the developed algorithm, we use the simple algebraic equations in a direct way without taking into account neither the number of levels nor the vectorial decomposition. The technique, which is developed in this paper, is general and simple. Moreover the computing time is independent of the number of levels and the quality of the obtained modulated voltage signals is very satisfactory.

5 Conclusion

A novel simple fast and general voltage space vector modulation system without Park transformation has been developed. The fundamental work is the modelling of the electric conversions of the $(n+1)$-level inverter using $2n$ three-level modulation functions. Then, the modulation waveform of the two reference line to line voltages has been copied onto output voltages of a three-phase multilevel inverter via an inversion of the modelling part. As a result, the proposed algorithm is generalized for any inverter levels. The validity of this algorithm is verified through simulations by considering a five-level DCI and an eleven-level DCI.

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