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The effects of the time-dependent and exposure time to air on Au/epilayer n-Si Schottky diodes

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Abstract. A study on Au/n-Si Schottky barrier diodes (SBDs) parameters with and without thin native oxide layer fabricated on n-type Si grown by LPE (Liquid-Phase Epitaxy) technique has been made. The native oxide layer with different thicknesses on chemically cleaned Si surface was obtained by exposing the Si surfaces to clean room air before metal evaporation. The native oxide thicknesses of samples D2, D3, D4 and D5 are in the form D2 < D3 < D4 ≤ D5 depending on the exposing time. It has been seen that the value of the barrier height Φ_b of samples D2 (0.64 eV), D3 (0.66 eV), D4 (0.69 eV) and D5 (0.69 eV) increases with increasing the exposure time and tends to that of the initial sample D1 (the initial sample, 0.74 eV), and thus also their $I-V$ curves. Especially, the experimental results related to the exposure time of the surfaces to clean air are close in agreement with recently results reported for the HF-treated n-Si surface during initial oxidation in air. Furthermore, it has been determined experimentally that ageing of the Au contacts on the oxidized epilayer Si leads to barrier height values close to those measured for Au on chemically cleaned surfaces.

PACS. 73.30.+y Surface double layers, Schottky barriers, and work functions – 73.40.Ns Metal-nonmetal contacts

1 Introduction

In the laboratory environment, crystal surfaces are usually covered with layers of native oxides and organic contaminants. It has been reported that the intrinsic surface states present at the semiconductor-vacuum interface before contact with the metal are an important factor in Schottky barrier formation [1–10]. In many cases, the barrier heights obtained on cleaved and chemically prepared semiconductor surfaces indicate the presence of an interfacial layer [1–10]. The effect of exposing cleaved and/or clean silicon surfaces to oxygen before forming the MS contacts has been investigated by many workers [7–15]. It is well-known that the interfacial layer thickness between metal and semiconductor is dependent on exposure time of the semiconductor surface to residual gases in the case of chemically cleaned substrates [4,5,16–20]. The layer-by-layer growth of the native oxide layer which is inevitably present on chemically prepared semiconductor surfaces thus occurs even when it is exposed to clean room air [4,5,16–20]. Archer and Atalla inspected the effect of exposing a cleaved surface to oxygen ambient for a few seconds before depositing the contact metal [8]. They found that the exposing to oxygen ambient for a few seconds is a negligible effect on the barrier height for Pt, Ni, Pd and Au, but a reduction of around 0.10 eV for Cu, Ag and Al. Turner and Rhoderick [9] estimated no difference in barrier heights on cleaved and etched surfaces for gold and nickel but a significant decrease on the etched surfaces for copper, silver and aluminum and they studied also the effect of ageing in Au/nSi diodes. Moreover, they [9] pointed out that ageing is important for metals on chemically etched surfaces and observed variations in the measured Schottky barriers of around 0.2 eV over a period of 1000 hours for Au contacts. In addition, the effect of the interfacial contamination in Au and Ag/atomically clean and oxidized silicon contacts were investigated by Varma *et al.* [10]. In their paper, it was reported that the contamination reduced the mechanical strength of adhesion between the MS interface. Furthermore, they reported that the barrier heights for gold and silver increased with time, ultimately yielding values close to those measured for intimate interfaces. Moreover, measurements of barrier heights on chemically etched silicon surfaces have also been made by several other workers, Kahng [11], Jäger and Kosak [12] and Hirose *et al.* [13]. Their results are generally similar to those of Turner and Rhoderick [9], although they did not study ageing effects. The ageing of gold and copper contacts on oxidized silicon has also been studied by Mothrom *et al.* [14]. For copper contacts, they found that the ageing

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increased the barrier heights and leads to values close to those measured for copper on clean surfaces. Therefore, the control of the native-oxide growth has received an increasing attention in recent years [16–20]. Furthermore, one of the most frequently used chemicals in electronics industry is hydrofluoric (HF) acid. HF removes thermal and native oxides and is therefore an essential processing step of device fabrication and in particular a basic component of all kinds of cleaning procedures. The further integration in microelectronic technologies requires preparation of defect-free and contamination-free thin-film structures [16–20]. Recently, Morita *et al.* [16] described the factors controlling the native oxide growth on Si surfaces (without any metal contact) in air and ultrapure water at room temperature. Gräf *et al.* [17] studied the immersion time depending influence of HF–H_2O_2 mixtures on the Si(100) and Si(111) surface by means of X-ray photoelectron spectroscopy and high regulation electron energy loss spectroscopy (HREELS). They reported that HF–H_2O_2 mixtures react in a different way on Si(100) and Si(111) surfaces. The Si(100) surface shows a higher overall oxygen coverage than Si(111) with a substantial higher amount of Si–O–Si bridge bonded oxygen and found that dihydride termination decreases with increasing H_2O_2 concentration and immersion time which indicates the formation of Si(111)-like facets. Dittrich *et al.* [18] and Angermann *et al.* [19] investigated the electronic properties (surface potential and surface state distribution) of the HF-treated Si surface by the pulsed surface photovoltage technique (SPV) during initial oxidation in air; the SPV measurement does not need any metal contact preparation. In their studies, it is shown that the kind of HF treatment strongly influences the concentration of extrinsic defects with a lower state of oxidation; and it was found that native-oxide growth is highly sensitive to the concentration of extrinsic defects directly after HF treatment. Later on, Ma and Eades [20] reported the results of wet cleaning of Si(111) wafer surface by using HF/NH_4F buffer solutions with different pH values. They concluded that the pH value of an HF solution does significantly affect the etching rate of the Si(111) surface and their SIMS analyses did indicate that a water rinse after HF-treatment significantly speeds up the oxidation of the passivated wafer surface.

As have been mentioned above, the understanding of the detailed mechanisms of the oxidation, reduction and etching processes involved in wafer cleaning is essential for high device yield. Moreover, after the device fabrication, its performance and stability depending on time is an important matter in the device manufacturing. Therefore, the purpose of this paper is to report the experimental results of the Au/n-Si Schottky diodes fabricated from the chemically cleaned n-type epilayer Si surface which are exposed to clean room air before metal evaporation, and the effect of the ageing in this diodes. It will be clearly seen from our experimental results that time-dependent, or ageing, effects are particularly important for metals on chemically etched semiconductor surfaces, It was fabricated five samples depending on exposure time to clean room air. The previously polished epilayer Si wafer was cleaned by using a traditional RCA clean with the final dip in diluted HF for 30 s.

2 Experimental procedure

The sample in this study consists of a 18 μm phosphorus-doped Si layer (2 Ω cm) grown by LPE (Liquid-phase Epitaxy) on a 0.01 Ω cm (antimony-doped) n^+ substrate (100). The wafer was chemically cleaned using the RCA cleaning procedure (*i.e.*, a 10 min boil in $NH_4 + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$) with the final dip in diluted HF for 30 s, and then rinsed in DI water with ultrasonic vibration and dried by high purity nitrogen. The ohmic contact on the back surface of the wafer was made by evaporating Au–Sb, then the wafer was cut into pieces of 5 × 5 mm^2. One of them was immediately inserted into the evaporation chamber to form intimate Schottky contacts. This sample will be called D1 or the initial sample in this paper. However, It has been reported that even if diodes made by cleaving in a stream of metal in high vacuum have a very thin effective native oxide layer [1–7]. Before Schottky contact formation, the front surface of one of the remaining pieces with ohmic contact was exposed to clean room air for one day at room temperature (sample D2) to obtain a native oxide layer on the clean Si surface (so as to observe non-ideality behavior due to the native interfacial layer); the third piece for three days (sample D3), the forth piece for a week (sample D4), and the fifth piece for two weeks (sample D5). An average temperature of 25 °C and an average humidity of 40% characterize the clean room air. The Schottky contacts were formed by evaporating Au as dots with diameter of about 1 mm onto all the sample surfaces. Thus, the Au/n-Si samples with and without the interfacial layer were obtained. Thickness of the Au film was about 1200–1500 Å. All evaporation processes were carried out in a turbo molecular fitted vacuum coating unit at about 10^{-6} mbar. In order to observe the effect of exposure time to clean room air, the current-voltage characteristics of the samples were measured using a HP 4140B picoampermeter immediately after fabrication of the Schottky contacts, at the room temperature and in the dark. Moreover, in order to observe the effect of the ageing, the measurements were also repeated 15, 30, 45 days after fabrication of the Schottky contacts.

3 Results and discussion

When the Schottky barrier diodes (SBDs) with a thin interfacial layer (MIS) is considered, it is assumed that the forward bias current of the device is due to thermionic emission current and it can be expressed as [5–7]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \qquad (1)$$

where

$$I_0 = AA^*\theta_n T^2 \exp\left(-\frac{q\Phi_b}{kT}\right), \qquad (2)$$

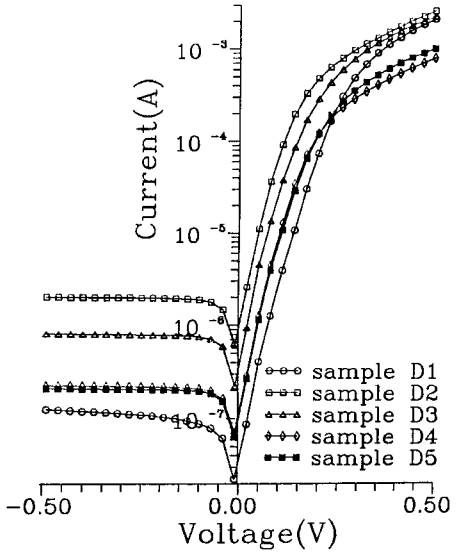

Fig. 1. Forward and reverse bias current *vs.* voltage characteristics of the Au/*n*-Si Schottky barrier diodes at the room temperature, the curve D1 corresponds to non-oxidized sample D1, and the curves D2, D3, D4 and D5 to samples D2 (exposed to air for one day), D3 (for three days), D4 (for 1 week) and D5 (for two weeks) with the interfacial native oxide layer.

is the saturation current density, $\Phi_{\rm b}$ is the barrier height at zero bias, A^* is the effective Richardson constant and equals to 112 A/cm^2 K^2 for n-type Si [3]; A the diode area; θ_n is the transmission coefficient the across the interfacial layer and it is given by $\theta_n = \exp\left(-(4\pi\delta/h)(2m^*\chi_{\rm c})^{1/2}\right)$, where m_n is the effective tunneling mass of electrons and $\chi_{\rm c}$ is the effective barrier height presented by the thin interfacial layer. If the interfacial layer is extremely thin and is transparent to electron, then $\theta_n \approx 1$. n is an ideality factor and is a measure of conformity of the diode to pure thermionic emission and is contained in the slope of the straight line region of the forward bias logarithm characteristics of I–V through the relation

$$n = \frac{q}{kT}\frac{{\rm d}V}{{\rm d}(\ln I)}\,. \qquad (3)$$

If n is equal to one, pure thermionic emission is occurring. However, n has usually a value greater than unity.

3.1 The parameters immediately after fabrication of the Schottky contacts or the effect of exposure time to air

The curves D2, D3 and D4 and D5 in Figure 1 show the experimental semilog forward and reverse bias I–V characteristics immediately after the fabrication of Schottky contacts the Au/n-Si. The barrier height value of Au/n-Si Schottky diodes were calculated with the help of equation (2) from the y-axis intercepts of the semilog-forward bias I–V plots, and the values of n were obtained using

Table 1. The experimental values of parameters obtained from I–V characteristics of the Au/n-Si diodes with and without the native oxide layer immediately and 45 days after fabrication of the Schottky contacts.

	immediately after		45 days after	
Diodes	n	$\Phi_{\rm b}$ (eV)	n	$\Phi_{\rm b}$ (eV)
D1	1.01	0.74	1.06	0.81
D2	1.02	0.64	1.06	0.77
D3	1.10	0.66	1.03	0.77
D4	1.10	0.69	1.12	0.81
D5	1.10	0.69	1.07	0.81

equation (3) from the linear region of these plots indicating that the series resistance effect in linear region is not important. The experimental values of the diode parameters immediately after fabrication of the Schottky contacts are given in Table 1. The $\Phi_{\rm b}$ value of 0.74 eV obtained for sample D1 is close to 0.75 eV obtained for evaporated Au on etched n-silicon [10]. As it can be seen in Table 1, the value of the barrier height $\Phi_{\rm b}$ for samples D2 (0.64 eV), D3 (0.66 eV), D4 (0.69 eV) and D5 (0.69 eV) with the interfacial layer increased with increasing the exposure time and tended to that of the initial sample D1 (0.74 eV). We can thus assume the sample D1 to have an ideal I–V characteristic with ideality factor value of 1.01. Furthermore, the ideality factor values of 1.06, 1.10, 1.10 and 1.10 for the samples D2, D3, D4 and D5, respectively, show that the devices do not obey an ideal Schottky diode behavior but a MIS configuration. In a such case, the interface states are in equilibrium with the semiconductor over the applied voltage range [1–22]. Thus, the non-ideal behavior due to the interfacial layer thickness may be described by an increase of n-value with increasing the oxide thickness. The concavity of the non-linear region in the forward ln(I–V) curves for the samples D2, D3, D4 and D5 increase with increasing the exposure time to the room air with respect to those of the initial sample D1. This indicates that the interfacial layer thickness increases with increasing exposure time.

The $\Phi_{\rm b}$ value of 0.74 eV for the initial sample D1, which is immediately inserted into the evaporation chamber without exposing to clean room air, is larger than those for the samples with the native oxide layer. This is attributed to the passivation of the cleaned Si surface after HF treatment. Hydrogen plays an important role for the electrical passivation of the HF-treated Si surface, is lower with respect to the trap passivation at the Si/SiO_2 interface [1–3,16–20,23–25]. As indicated in references [16–20,23–25], immediately after the HF treatment shows a predominant coverage of the surface with hydride groups. That is, Si atoms at the cleaned Si wafer surface are terminated by hydrogen. As known, the intrinsic surface states present at the semiconductor-vacuum interface before contact with the metal are an important factor in Schottky barrier formation or Fermi level pinning at the interface. These intrinsic surface states may be passivated by means of HF treatment.

Moreover, as it can be seen in Table 1, the Φ_b value of 0.64 eV for sample D2 is lower than those for the samples D3, D4 and D5. This may also be ascribed to oxygen species that break Si–Si bonds to produce Si–O–H bonds, with the remaining Si–H bonds to cause hydrophobic behavior [16–20]. That is, HF induced extrinsic states decrease after an initial phase of 24 h, while an other group of the extrinsic states additionally appears such as Si–O bonds; and their maximum concentration reached after 7 days is followed by a slow decrease during further exposure to air [16–20]. As has previously been observed by Archer and Atalla [8], Turner and Rhoderick [9] and Aboelfotoh [26], the barrier height value is lower for the relatively thin interfacial oxide layer (the sample D2 with respect to the samples D3, D4 and D5). That is, the data show that the relatively thin oxide layer on the initial Si(100) surface (the sample D2 with respect to the initial sample D1) are sufficiently to cause a decrease in n-type barrier height of about 0.10 eV, or to shift the Fermi level above the gap center. Aboelfotoh [26] found that only a few (2–3) monolayer on the Si(100) surface causes a decrease in the barrier height of about 0.12 eV for Ti/n-Si Schottky diodes. Archer and Atalla [8] found that the exposing to oxygen ambient for a few seconds is a reduction of around 0.10 eV for Cu, Ag and Al. Turner and Rhoderick [9] obtained a significant decrease on the etched surfaces for copper, silver and aluminum due to small effect of air exposure for the barrier height. Again, as indicated in references [16–20,23–25], on a hydophobic surface, the development of an oxygen coverage during subsequent storage in air occurs extremely slowly. In study on oxidation of HF-treated Si wafer surfaces in air by Gräf *et al.* [23], a monolayer coverage of oxygen is reached after approximately 7 days.

Likewise, the behavior of Φ_b with increasing exposition time in air may be explained as follows: during further storage in air, the oxygen species are produced at native oxide surfaces by the coexistence of O_2 and H_2O. The Si–Si bonds of the underlayer Si are broken to produce Si–O bonds after all of the Si atoms in the overlayer are oxidized [16]. Thus the surface state distribution becomes more and more like a Si/SiO_2 interface after long exposure to air. However, it has been showed the results of references [23–25] that the oxide on hydrophobic surface consists of hydrated SiO_2 through all stages of the growth in the air. Therefore, the stabilization of the structures ascribed to the passivation of the interface by hydrogen and oxygen The stabilization of the interface is also confirmed with the identical ideality factor value of 1.10 for samples D3, D4 and D5, respectively. This case is in agreement with experimental results reported by the pulsed surface photovoltage (SPV) technique [18,19] used to examine the electronic properties of the HF-treated Si surface during initial oxidation in air. Thus, it has been said that the barrier height of Au on the relatively thick silicon oxide covered silicon surfaces, where the wave functions of the metal electrons are likely to be decoupled from those of the semiconductor, appears to be in good agreement with the simple Schottky picture.

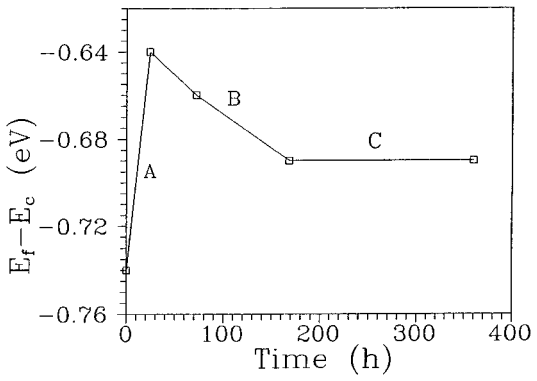

Fig. 2. The Fermi level position at the interface as a function of exposure time to clean air for the wafers at room temperature.

It is well-known that the barrier formation is related to the pinning of Fermi level at the interface due to the interface states or interfacial insulating layer. Therefore, the shift of Fermi level position E_f at the interface with respect to the top of the conduction band at the surface of the n-type semiconductor should (the plotting $E_f - E_c$ *vs.* time) be shown as a function of exposure time to air. Figure 2 shows the Fermi level position (at the surface) as a function of exposure time of the wafers to air at room temperature. This figure was drawn with the help of the barrier height values obtained from the forward I–V characteristics of the samples. The exposure time ranges from 24 h (1440 min) to 336 h (20 160 min). There are three regions in the figure. We connect the region A to the initial oxidation (which is characterized by replacement of Si–H by S–O–H) and the region B to the formation of a Si/SiO_2 interface (the electronic properties of the surface change drastically). However, according to results of references [23–25], even after storage times longer than about two weeks, Si–H groups are still present. Thereby, we connect region C to the stabilization of the Si/SiO_2 interface as well as the passivation of the Si surface by hydrogen (the electronic properties are similar to the Si/SiO_2 interface), depending on the above explained dynamics. In addition, the region A which corresponds to the degrease of the barrier height from 0.74 eV for D1 to 0.64 eV for D2 can be due to small effects of O_2 and air exposure on the barrier height, as mentioned in references [8,9,23]. The change in the Fermi level position in the exposure time range 24–336 h is in agreement with results determined by pulsed surface photovoltage technique in Figure 4 of reference [18].

In conclusion, the I–V characteristics and experimental parameters of the Au/n-Si SBDs are in agreement with experimental results reported by the pulsed surface photovoltage technique (SPV). It has been seen that the characteristics parameters of samples D2, D3, D4 and D5 have increased with increasing exposure time to room air and that the I–V and Φ_b values tended to those of sample D1. Furthermore, the above results are related to the measured parameters immediately after fabrication of the Au Schottky contacts on the epilayer Si that are exposed to room air without considering the change of the native

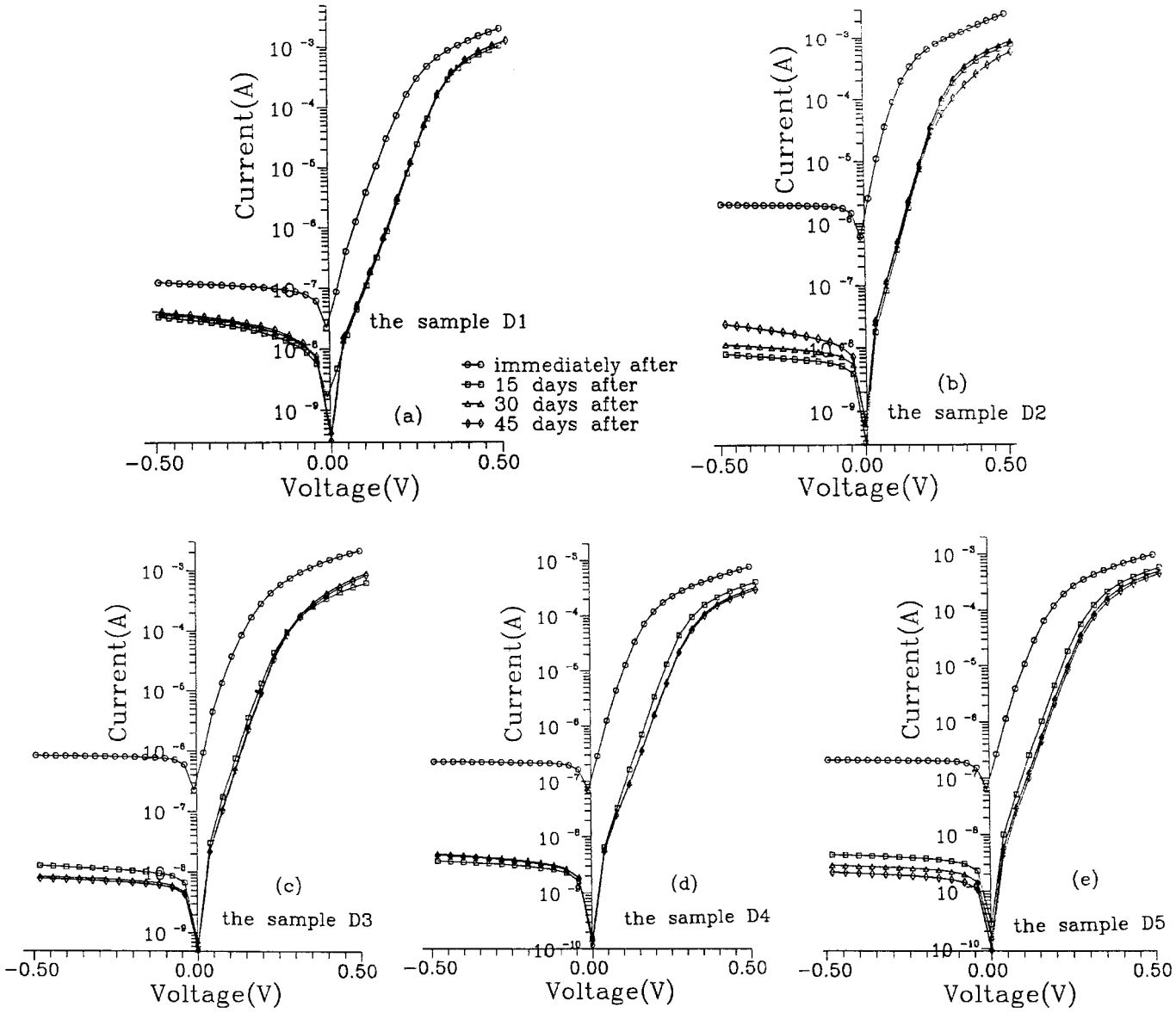

Fig. 3. *I–V* characteristics of the Schottky diodes (the samples D1, D2, D3, D4, D5) with the ageing as parameter at room temperature. (a) The sample D1, (b) the sample D2, (c) the sample D3, (d) the sample D4, (e) the sample D5.

oxide layer between the Au and Si depending on time (the effect of ageing).

3.2 The effect of the ageing

Time-dependent, or ageing, effects are particularly important for metals on chemically etched semiconductor surfaces, as pointed out by Turner and Rhoderick [9]. Figure 3 show the *I–V* curves measured immediately, 15 days, 30 days and 45 days after fabrication of the Schottky contacts for all the diodes. The Fermi level position as a function of the ageing of the Schottky diodes at room temperature is shown in Figure 4. The parameters related to the ageing are given in Table 1.

It can be seen from Figure 4 that the ageing increases the barrier heights and leads to value of about 0.81 eV measured for gold on chemically prepared clean surfaces and on cleaved surfaces [9,10]. When the ageing was completed, the equilibrium value of Φ_b was found to depend on the exposing time of the surfaces to clean room air before evaporating metal. These observations can be explained in terms of the existence of a thin oxide layer on the chemically prepared surfaces. For example, the sample D1 reached the equilibrium barrier value 15 days after metal deposition while the samples D2 and D3 reached it after 30 days and samples D4 and D5 after 45 days. This seems to be associated with some low change in the oxide film depending on the exposing time of the surfaces (that is, depending on the oxide layer thickness). It can be said that the steady value is reached when dipole between the metal and semiconductor which would modify the barrier height disappears. As was suggested in references [2,5,9],

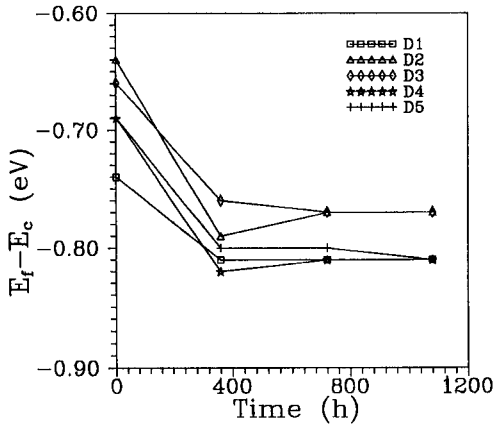

Fig. 4. The Fermi level position as a function of the ageing of the Schottky diodes (the samples D1, D2, D3, D4, D5) at room temperature. The curve D1 corresponds to the initial sample D1, and the curves D2, D3, D4 and D5 to samples D2 (exposed to air for one day), D3 (for three days), D4 (for 1 week) and D5 (for two weeks) with the interfacial native oxide layer.

the ageing process is similar in nature to the ageing of MOS structures. The time scale of the ageing suggests an ionic activity within the oxide film rather than an electronic activity and it can be attributed to the migration of charged ions through the oxide layer. During the migration, the ions, together with the compensating charges on the surface of the metal, would give rise to a dipole which would modify the barrier height. The dipole would disappear when the ions reach the metal and their charge is neutralized and the equilibrium barrier value will be thus reached. This explanation of the ageing is consistent with our experimental measurement.

As it can be seen from Figure 3 and Table 1, an equilibrium barrier height value of about 0.81 eV for the samples D1, D4 and D5 (Au/epilayer n-Si) was obtained, and a value of about 0.77 eV for the samples D2 and D3. Thus, we observed variations in the measured Schottky barriers of about 0.07 eV for the sample D1, 0.13 eV for the samples D2, 0.11 eV for the sample D3, 0.12 eV for the samples D4 and D5 over a period of 1080 hours. Turner and Rhoderick [9] observed a variation of around 0.2 eV over a period of 1000 hours for Au/n-Si Schottky diodes. Likewise, Mothrom *et al.* [14] studied the ageing of gold and copper contacts on oxidized silicon and found that for Cu the ageing increases the barrier heights up to values close to those measured for copper on clean surfaces. The equilibrium barrier height value of 0.81 eV for the initial sample is exactly in agreement with the value of 0.81 eV obtained for cleaved surface by Archers and Atalla [8] and Turner and Rhoderick [9], and for chemically prepared surfaces by Turner and Rhoderick [9] in Au/n-Si Schottky diodes. As it can be seen in Table 1, when considering the ideality factor values 45 days after (1080 h), it increases by 0.05 for the sample D1, by 0.04 for D1 and by 0.02 for the D4, and it decreases from 1.10 to 1.03 and 1.07 for the samples D3 and D5. The ideality factor values in Au/n-Si Schottky diodes etched using HF/HNO_3 (1:8) by Turner and Rhoderick [9] (initial value of 1.08) changed between 1.15 and 4 over a period of 1000 hours.

Briefly, it was found experimentally that the ageing of the Au contacts on the oxidized epilayer Si increased the barrier heights leading to values close to those measured for Au on chemically clean epilayer Si surfaces. On the other hand, for the relatively thin interfacial oxide layer, the barrier height value is lower. Although the barrier height of Au on the relatively thick silicon oxide covered silicon surfaces (the samples D4 and D5), where the wave functions of the metal electrons are likely to be decoupled from those of the semiconductor, appears to be in good agreement with the simple Schottky picture (the sample D1), the value for the passivated silicon surfaces is also within the experimental accuracy expected for this model.

References

1. J. Brillson, Sur. Sci. Rep. **2**, 123 (1982).
2. E.H. Nicollian, A. Goetzberger, Bell. Syst. Tech. J. **46**, 1055 (1986).
3. J.H. Werner, U. Rau, *Springer Series in Electronics and Photonics*, edited by J.F. Luy, P. Russer (Sipringer, Berlin, 1994), Vol. 32.
4. A.M. Cowley, S.M. Sze, J. Appl. Phys. **36**, 3212 (1965) .
5. H. Rhoderick, R.H. Williams, *Metal-Semiconductor Contacts* (Clarendon, Oxford, 1988), pp. 73, 99.
6. A. Türüt, B. Batı, A. Kökçe, M. Sağlam, N. Yalçın, Phys. Scr. **53**, 118 (1996).
7. H.C. Card, E.H. Rhoderick, J. Phys. D **4**, 1589 (1971).
8. J. Archers, M.M. Atalla, Am. Acad. Sci. N.Y. **101**, 697 (1993).
9. M.J. Turner, E.H. Rhoderick, Solid-State Electron. **11**, 291 (1968).
10. R.R. Varma, A. McKinley, R.H. Williams, J.G. Higginbotham, J. Phys. D: Appl. Phys. **10**, L171 (1977).
11. D. Kahng, Solid-State Electron. **10**, 45 (1963).
12. H. Jäger, W. Kosak, Solid-State Electron. **12**, 511 (1969).
13. M. Hirose, N. Altaf, T. Aruzimi, Jpn J. Appl. Phys. **9**, 270 (1970).
14. J.D. Mottrom, D.C. Nothrop, C.M. Reed, A. Thanailakis, J. Phys. D: Appl. Phys. **12**, 773 (1979).
15. R.S. Bauer, R.Z. Bachrack, L.J. Brillson, Appl. Phys. Lett. **37**, 1006 (1980).
16. M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, M. Ohwada, J. Appl. Phys. **68**, 1272 (1990).
17. D. Gräf, S. Bauer-Mayer, A. Schnegg, J. Appl. Phys. **74**, 1679 (1993).
18. Th. Dittrich, H. Angermann, W. Füssel, H. Flietner, Phys. Stat. Sol. **140**, 463 (1993).
19. H. Angermann, Th. Dittrich, H. Flietner, Appl. Phys. A **59**, 193 (1994).
20. Y. Ma, J.A. Eades, Appl. Phys. A **62**, 247 (1996).
21. A. Türüt, N. Yalçın, M. Sağlam, Solid-State Electron. **35**, 835 (1992).
22. A. Singh, Solid-State Electron. **28**, 233 (1985).
23. D. Gräf, M. Grundner, R. Schulz, L. Mühlhoff, J. Appl. Phys. **68**, 5155 (1990).
24. M. Grundner, H. Jacob, Appl. Phys. A **39**, 73 (1986).
25. B.R. Weinberger, G.G. Peterson, T.C. Eschrich, H.A. Krasinski, J. Appl. Phys. **60**, 3232 (1986).
26. M.O. Aboelfotoh, Phys. Rev. B **39**, 5070 (1989).