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PSPICE model of the power LDMOS transistor for radio frequency applications in the 1.8−2.2 GHz Band

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Abstract. In this paper, we propose a model for the LDMOS transistor used for power amplification in the frequencies band 1.8–2.2 GHz dedicated to the mobile telephony system Digital Cellular System (DCS). This model takes into account the behaviour of each internal region of the power structure. A new representation of the non-linear inter-electrode capacitances, drain-gate C_{gd} and drain-source C_{ds}, is proposed. The obtained model is implemented in the circuit simulator PSPICE, which gives an overall evaluation of the transistor performances in the radio frequency power amplification mode. This model is mainly intended to the system designer. A study of the power amplification in the SHF band at 2 GHz is performed. A good agreement between experimental and simulation results is found.

PACS. 73.40.Qv Metal-insulator-semiconductor structures (including semiconductor-to-insulator)

1 Introduction

The progress recently made in MOS transistors technology has led to the realisation of a new generation of LDMOS structures [1–4] which may be used for radio frequency power amplification in the frequencies band 1.8–2.2 GHz allocated to the DCS system for mobile radio telephony. The LDMOS offer the same intrinsic advantages as the vertical VDMOS transistors [5–8], *i.e.* high power gain, good linearity, absence of hot spot and good thermal stability. These power LDMOS transistors are used in the output stages of the base station transmitter having an output power up to 120 W. In order to achieve such an emission power, several transistors are connected in parallel.

In this paper, our main objective is to build a model for the SHF power LDMOS transistor. The complete development of the equivalent circuit is based on the analysis of each internal region of the structure. Subsequently, an original model for the non-linear inter-electrode capacitances, gate-drain C_{gd} and drain-source C_{ds}, as well a method for implementing in the PSPICE circuit simulator [9] are presented and validated. The proposed model is intended to the system designer. In the power amplification mode, the validation of the model is carried out for a working frequency of 2 GHz.

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2 SPICE model of the SHF LDMOS transistor

Figure 1 shows a schematic cross-section of the LDMOS structure for radio frequency power amplification applications [1–4]. The three electrodes are interdigited and form parallel bands distributed into cells [2]; each cell contains several elementary transistors, *i.e.* fingers (Fig. 1). Figure 2 shows a microphotography of the radio frequency power LDMOS transistor used in the study [3].

The equivalent electric circuit is obtained by an analysis of each internal zone of the transistor. We treat successively the channel, the drift and the gate regions.

2.1 Equivalent circuit in the static mode

Channel region

A controlled current generator described by the MOS transistor "level 3" in the SPICE library [9] may model the channel active zone. In the ohmic conduction mode, the current expression J_d is:

$$J_d = K_p \left[(V_g - VT)Vd - (1 + FB)\frac{Vd^2}{2} \right]$$

$$\text{with} \qquad K_p = \mu_{eff} \frac{W}{L} C_{ox} \tag{1}$$

where W and L are respectively the width and the length of the channel, C_{ox} the gate oxide capacitance per area

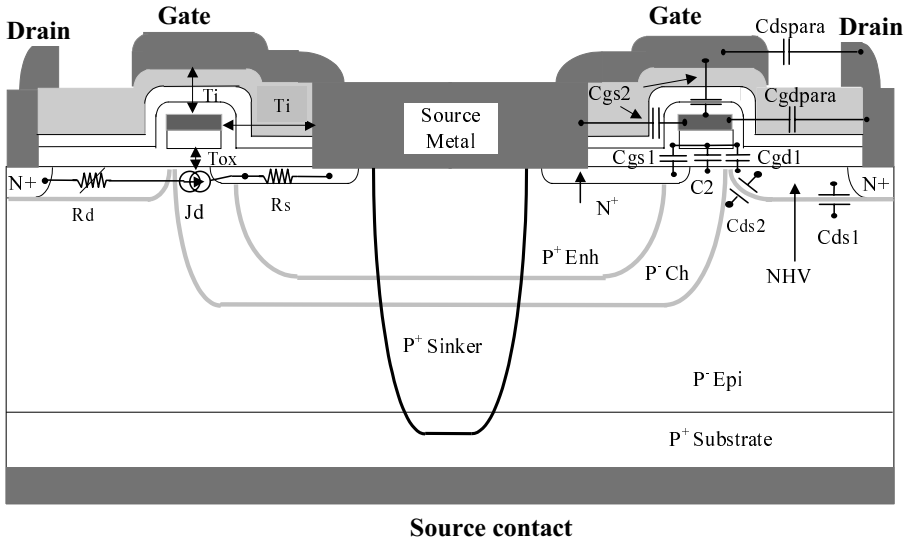

Fig. 1. Schematic cross-section (AA') of two elementary fingers of the SHF radio frequency LDMOS transistor.

unit, V_d the voltage across the channel, VT the threshold voltage, V_g the gate internal voltage, FB an expression which accounts for the effects of short channel and narrow channel. The carrier mobility in the channel inverted layer μ_{eff} depends on the longitudinal and transversal components of the electric field. It is given by [9]:

$$\mu_{eff} = \frac{\mu_s}{1 + \dfrac{\mu_s V_d}{V_{max} L}} \quad \text{with} \quad \mu_s = \frac{\mu_0}{1 + \Theta(V_g - VT)} \qquad (2)$$

where μ_0 is the low field carriers mobility, V_{max} the limit velocity of the carriers. μ_s is the surface carrier mobility in the channel inverted layer, it depends on the transverse component of the electric field (roll-off coefficient Θ).

In the pinched mode, the perfect saturation hypothesis, giving rise to a horizontal output characteristic, is justified by the fact that the structure has a less doped drain than the channel diffusion, *i.e.* the modulation of the channel length is negligible.

Drift region

Several studies made on power LDMOS transistors [10,11] have shown that the drift region of the lowly doped drain present a variable resistance which mainly depends on the drain bias. Figure 3 shows the on-state resistance Ron variation with respect to the drain voltage; VGS is maintained constant equal to 10 V. Under such high voltage, Ron may be reduced to the resistance of the drift region Rd [12] as the resistances of the channel and the accumulation region can be neglected. We notice that Rd is linearly raising with respect to VDS. The increases of Rd give rise to more pronounced curvatures on the output characteristics IDS (VDS), especially when the gate voltage is high. This phenomenon known as quasi-saturation [10,11] may be interpreted as the non-linear dependence of the carrier velocity *versus* the high value of the electric field due to the short length of the drift zone. In the new

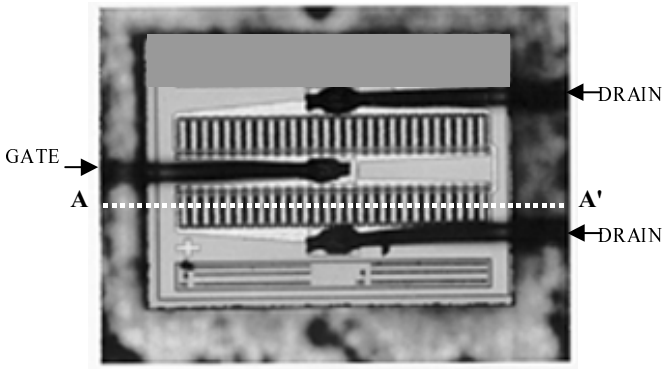

Fig. 2. Microphotography of the SHF LDMOS transistor (two cells, 3 W at 2 GHz).

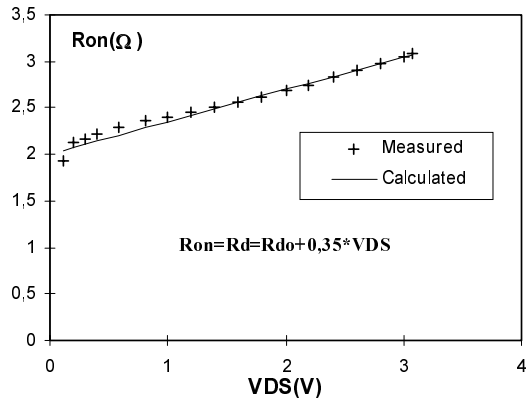

Fig. 3. Typical variations of the on-state resistance with respect to the drain bias, at $VGS = 10$ V.

generation of radio frequency LDMOS structures [2,3], an n-type diffusion (NHV) extends from the drain diffusion to the channel (Fig. 1). This minimises the quasi-saturation effect. In the simulator PSPICE, the non-linear drift

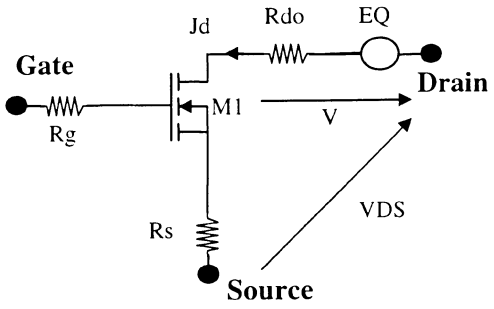

Fig. 4. Equivalent circuit in the static mode of the SHF LDMOS.

resistance R_d is modelled by an equivalent circuit formed by a constant resistance R_{do} in series with a voltage source EQ which depends on VDS "$EQ = \gamma VDSJ_d$" [10] (Fig. 4). The voltage drop across the drift resistance is given by:

$$V = R_{do}J_d + EQ = R_{do}J_d + \gamma VDSJ_d. \quad (3)$$

In the static mode, the transistor equivalent circuit is completed by the parasitic resistances R_g and R_s located respectively on the gate and the source electrodes (Fig. 4).

The experimental procedures for finding the main parameters intervening in the static mode equations are given elsewhere [13]. A special care is taken for the coefficient K_p (Eq. (1)) which is inferred from a measurement of the transfer characteristic slope at low level. Those parameter values are summarised in Table 1.

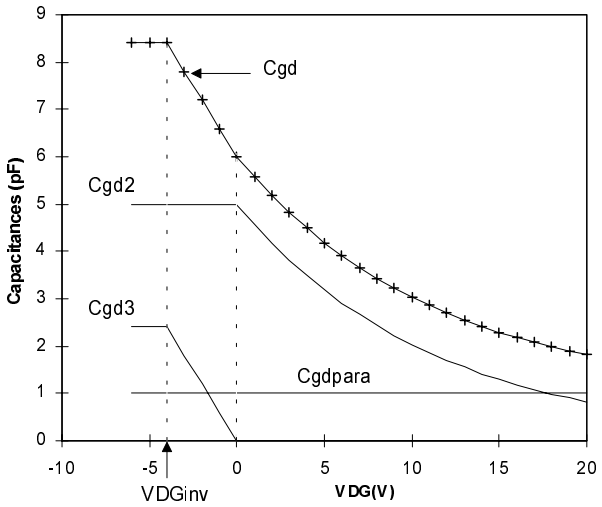

Fig. 5. Typical variation of the "reverse" capacitance C_{gd}.

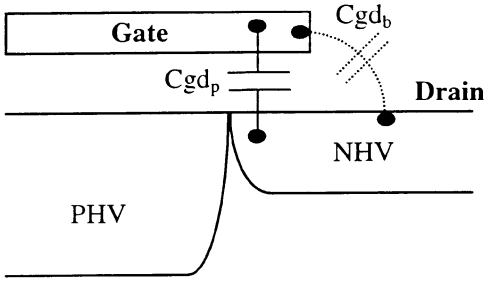

Fig. 6. Components of the capacitance C_{gd1}.

2.2 Equivalent circuit in the dynamic mode

When the transistor is operating in the dynamic mode, the added internal elements to be taken into consideration are mainly [14] the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd} and the drain-source capacitance C_{ds}.

Gate-source capacitance

The gate-source capacitance (Fig. 1) consists of:

- C_2: the thin oxide gate capacitance, located between the gate and the channel diffusion. Its value varies according to the DC bias conditions between $\frac{2}{3}WLC_{ox}$ and WLC_{ox}. We assume for the model that C_2 is constant and equal to the maximum value;
- C_{gs1}: the capacitance due to the covering of the gate over the diffusion N^+ of the source;
- C_{gs2}: the capacitance due to the covering of the source metallization over the gate.

The capacitances C_2, C_{gs1} and C_{gs2} depend on physical and geometrical quantities (oxide permittivity, thin and thick oxide thicknesses and the component geometry) and are given by:

$$C_{gs1} = \frac{\varepsilon_0\varepsilon_{ox}}{T_{ox}}S_1 \quad C_{gs2} = \frac{\varepsilon_0\varepsilon_{ox}}{T_i}S_2 \quad C_2 = \frac{\varepsilon_0\varepsilon_{ox}}{T_{ox}}S_3 \quad (4)$$

where S_1, S_2 and S_3 are the respective area, depending on the transistor geometry. T_{ox} is the gate oxide thickness, T_i the oxide thickness between the gate and the source metallization (Fig. 1).

Gate-drain capacitance C_{gd}

The capacitance between the gate and the drain has a strong non-linear behaviour (Fig. 5). This capacitance is made up by a constant capacitance C_{gdpara} between the gate and the drain plating and a non-linear capacitance C_{gd1} between the gate and the drift diffusion NHV (Fig. 1).

C_{gdpara} is constant and can be identified to C_{gd} when VDG is high, typically in order of 100 V near the breakdown voltage VBR

$$C_{gdpara} = C_{gd}(VDG \to VBR). \quad (5)$$

The capacitance C_{gd1} is a combination of two elements (Fig. 6):

(i) the MOS capacitance C_{gdp} of the plane region due to the covering of the gate over the drift diffusion NHV;
(ii) the parasitic capacitance C_{gdb} due to the edge effect. As the gate overlap is small, the part C_{gdb} contribution is not negligible compared to the part C_{gdp}.

Table 1. Model element values for the studied transistor.

Static parameters			
K_p (A/V^2)	VTO (V)	$THETA$ (V^{-1})	V$_{MAX}$ (m/s)
0.2	3.1	0.3	12 10^5
R_g (Ω)	R_s (Ω)	R_{do} (Ω)	γ
1	0.001	0.11	0.05

Dynamic parameters							
C_{gd} (pF)						C_{ds} (pF)	
τ_{gd}	C_{jogd}	α	VDG_{inv} (V)	C_{gdpara}	C_{jods}	τ_{ds}	C_{dspara}
0.16	0.848	-0.28	-1.6	0.1	5.29	0.3	0.4
C_{gs} (pF)		L_g (nH)		L_s (nH)		L_d (nH)	
7.8		0.1		0.1		0.1	

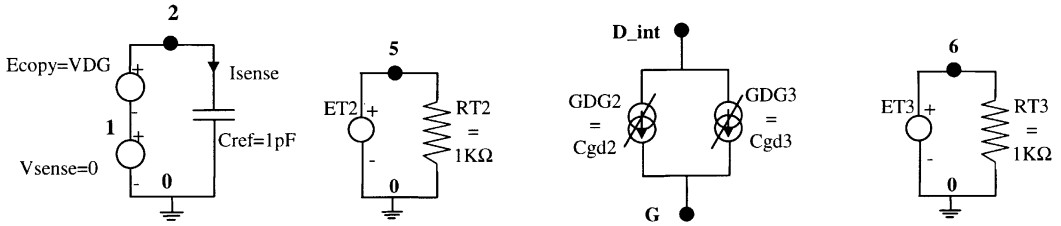

Fig. 7. Modelling of the capacitances C_{gd2} and C_{gd3} in PSPICE.

For this reason, the capacitance C_{gd1} can not be modelled by the transition capacitance of a reverse biased pn junction as it was proposed for the power VDMOS transistor [15]. We suggest representing C_{gd1} by two non-linear capacitances (C_{gd2} and C_{gd3}) which are functions of the voltage across their terminals, given by the empirical equations:

$$\begin{cases} C_{gd2}(VDG) = C_{jogd}e^{(-\tau_{gd}VDG)} & \text{when} \quad 0 \le VDG \le 100 \\ C_{gd2}(VDG) = C_{jogd} & \text{when} \quad VDG \le 0 \end{cases} \tag{6}$$

C_{jogd} and τ_{gd} are extracted from the experimental curve $C_{gd}(VDG)$:

$$C_{jogd} = C_{gd}(0) - C_{gd}(VDG \to VBR) = C_{gd}(0) - C_{gdpara}$$

$$\tau_{gd} = \frac{1}{VDG}\ln\left(\frac{C_{jogd}}{C_{gd}(VDG)}\right)$$

$$\begin{cases} C_{gd3}(VDG) = -\alpha VDG_{inv} \ \text{ when } \ VDG \le VDG_{inv} \\ C_{gd3}(VDG) = -\alpha VDG \ \text{ when } \ VD_{Ginv} \le VDG \le 0 \\ C_{gd3}(VDG) = 0 \ \text{ when } \ VDG \ge 0 \end{cases} \tag{7}$$

with

$$\alpha = \frac{C_{gd}(VDG_{inv}) - C_{gd}(0)}{VDG_{inv}} \cdot$$

The implementation of these non-linear capacitances in the "Analog Behavorial" modelling syntax of PSPICE is not straightforward. They are introduced by using the controlled current source element [16]. The circuit used for implementing C_{gd2} and C_{gd3} is shown in Figure 7. The voltage generator Ecopy is used for reproducing the instantaneous current I_{sense} induced by the voltage variations VDG through a constant capacitance C_{ref}. The voltage source of null value V_{sense} is used to sense this capacitive current. The current crossing C_{ref} may be written as:

$$I_{sense} = C_{ref}\frac{dE_{copy}}{dt} = C_{ref}\frac{dVDG}{dt} \cdot \tag{8}$$

In PSPICE, due to the possibility offered by the command TABLE, the voltages $V(5,\,0)$ and $V(6,\,0)$ of the nodes 5 and 6, with respect to the ground, depend on VDG by:

$$\begin{cases} V(5,0) = 100 & \text{when} \quad VDG \ge 100 \\ V(5,0) = VDG & \text{when} \quad 0 \le VDG \le 100 \\ V(5,0) = 0 & \text{when} \quad VDG \le 0 \end{cases}$$

$$\begin{cases} V(6,0) = 0 & \text{when} \quad VDG \ge 0 \\ V(6,0) = VDG & \text{when} \quad VDG_{inv} \le VDG \le 0. \\ V(6,0) = VDG_{inv} & \text{when} \quad VDG \le VDG_{inv} \end{cases} \tag{9}$$

The expression of the currents I_{dg2} and I_{dg3} of the controlled current sources $GDG2$ and $GDG3$ is:

$$I_{gd2} = \frac{C_{jogd}}{C_{ref}} e^{(-\tau_{gd} V(5,0))} I_{sense}$$
$$= C_{jogd} e^{(-\tau_{gd} VDG)} \frac{dVDG}{dt} = C_{gd2} \frac{dVDG}{dt} \quad (10)$$
$$I_{gd3} = -\frac{\alpha V(6,0)}{C_{ref}} I_{sense}$$
$$= -\alpha VDG \frac{dVDG}{dt} = C_{gd3} \frac{dVDG}{dt} \cdot \quad (11)$$

The currents I_{gd2} and I_{gd3} are the instantaneous currents which flow through the capacitances C_{gd2} and C_{gd3}. In order to ensure the validity of expressions (Eqs. (6, 7)), the command TABLE (Eq. (9)), control the variation ranges for the gate-drain voltage.

pn *junction capacitance* C_{ds}

In the normal mode ($VDS > 0$), the junction formed by the epitaxy P^-Epi and the drift diffusion NHV is always reverse biased. The associated capacitance is made of two components (Fig. 1):

(i) the transition capacitance of the plane region C_{ds1};
(ii) the cylindrical region capacitance C_{ds2}.

In the radio frequency power LDMOS transistors, the value of C_{ds} is small but the contribution part of the cylindrical region capacitance is not negligible in contrary to the power VDMOS transistor case. Therefore, the transition capacitance relationship of a reverse biased *pn* junction as implemented in SPICE is insufficient to correctly model C_{ds}. In order to account for the experimental evolution of C_{ds} with respect to the dynamic voltage VDS, we propose an empirical equation like the capacitance C_{gd} case

$$C_{ds}(VDS) = C_{jods} e^{(-\tau_{ds} VDS)} + C_{dspara}$$
$$\text{when} \quad VDS \geq 0 \quad (12)$$

with

$$C_{dspara} = C_{ds}(VDS \to VBR)$$
$$C_{jods} = C_{ds}(0) - C_{dspara}$$
$$\tau_{ds} = \frac{1}{VDS} \ln\left(\frac{C_{jods}}{C_{ds}(VDS) - C_{dspara}}\right) \cdot$$

The implementation of C_{ds} undergoes the same procedure as it was done above for C_{gd}. The current I_{ds} supplied by the controlled current source GDS is given by:

$$I_{ds} = \left(\frac{C_{jods}}{C_{ref}} e^{(-\tau_{ds} V(7,0))} + \frac{C_{dspara}}{C_{ref}}\right) I_{sense}$$
$$= (C_{jods} e^{(-\tau_{ds} VDS)} + C_{dspara}) \frac{dVDS}{dt} = C_{ds} \frac{dVDS}{dt} \cdot \quad (13)$$

The experimental determination of the parameter values associated with the capacitances is carried out by the measurement of the following capacitances:

(i) input C_{iss} with short circuited output;
(ii) output C_{oss} with short circuited input;
(iii) reverse capacitance C_{rss}.

The values of the inter-electrode gate-source, gate-drain and drain-source capacitances are calculated from the following relations:

$$C_{iss} = C_{gs} + C_{gd}, \quad C_{oss} = C_{ds} + C_{gd}, \quad C_{rss} = C_{gd}. \quad (14)$$

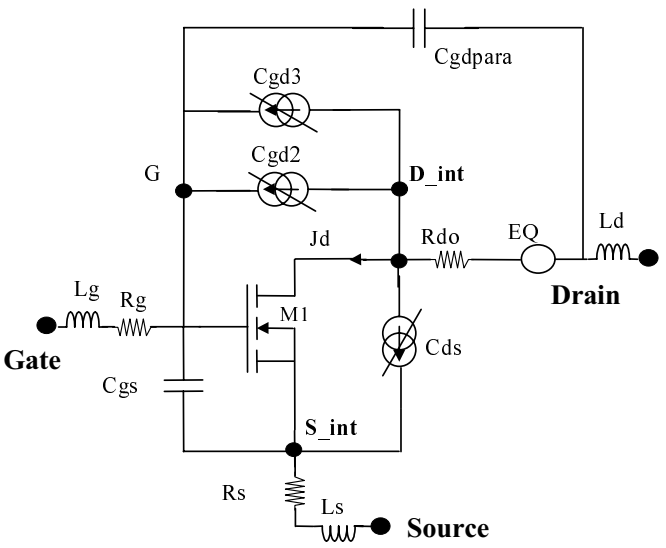

Fig. 8. Equivalent circuit of the SHF LDMOS transistor implemented in PSPICE.

Equivalent circuit

The inductances L_s, L_g, and L_d, associated with respectively the source, the gate and the drain electrodes, are introduced for accounting the parasitic elements of the die packaging. The final equivalent circuit (Fig. 8) can be used for the simulation of the main interesting modes of operation, static, switching on the resistive and inductive load and large signal amplification in the SHF band.

Figures 9 to 11 show a comparison between measured inter-electrode capacitances and those obtained with the simulation. For C_{gd} and C_{ds}, the comparison is carried out with the "classical" model of a reverse biased *pn* junction capacitance [15] and also with the proposed model. The actual follows accurately the measurement results.

3 Model validation in the static mode

The example shown in Figure 12 makes it possible to appreciate the precision degree of the model, which mainly was obtained by considering the mobility reduction phenomenon in the channel active zone and in the drift region NHV. Let us notice that in the new generation of LDMOS structures, the quasi saturation effect is reduced with

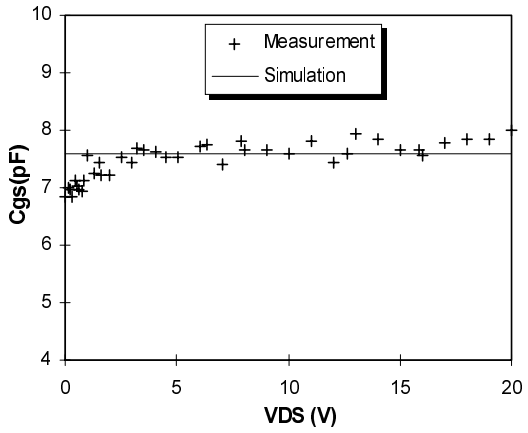

Fig. 9. Variations of the gate-source capacitance with respect to the drain-source voltage.

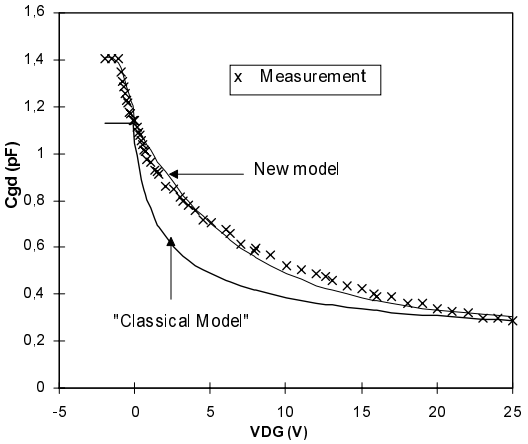

Fig. 10. Variations of the gate-drain capacitance with respect to the drain-gate voltage at $VGS = 0$ V.

respect to the classical power LDMOS structures used for switching applications [12]. Indeed, in the classical LDMOS transistors, the carriers cross a weakly doped layer N^-, which is very short and where the electric field is high.

4 Validation in the radio frequency power amplification mode

In the purpose to validate the RF model, some results obtained with a one-stage amplifier are presented here. The set made use of matching networks, tuned at 2 GHz for a bias current I_{DS0} of 50 mA (class AB), and embedded in the design of the amplifier printed board. This bias point is chosen as it maximises the flatness range of the power gain. Results are also presented for two other cases: a doubled bias current class AB operation; *i.e.* $I_{DS0} =$ 100 mA; and a class C operation; at $VGS = 0$ V ($I_{DS0} =$ 0 A). As the matching networks can not be re-tuned on the board, this study part aims to test the model validity range, *i.e.* out of adjusted impedance matching operation.

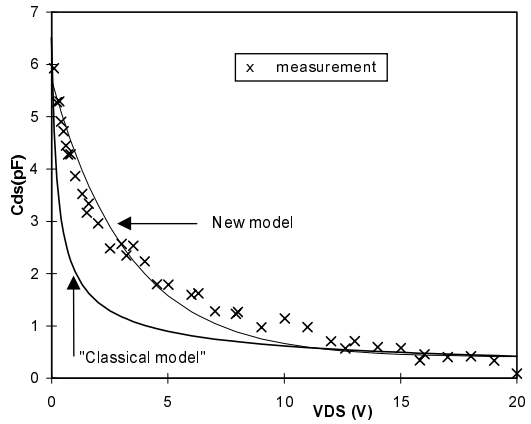

Fig. 11. Variations of the drain-source capacitance with respect to the drain-source voltage.

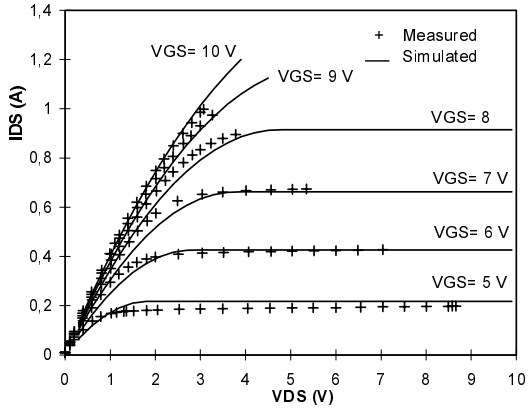

Fig. 12. Static output characteristics of the SHF LDMOS transistor.

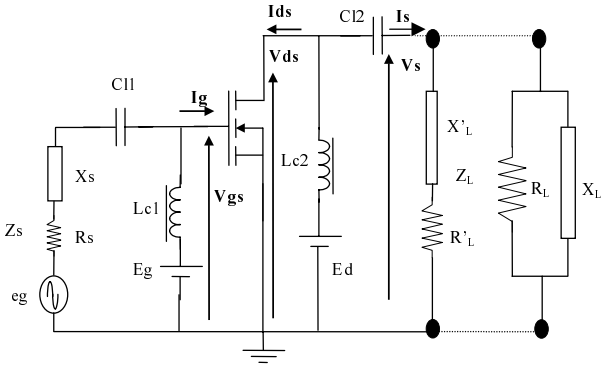

Fig. 13. Radio Frequency amplifier circuit as it is implemented in PSPICE.

In the other hand, the circuit implemented in the simulator PSPICE, which is used to theoretically determine the narrow band radio frequency performances, is shown in Figure 13. The circuit is made up by the LDMOS equivalent circuit, the drain and gate DC bias circuits, and the passive circuits for input and output impedance matching, respectively Z_S and Z_L. The input network is formed by a real part R_S in series with an imaginary part X_S; the output network may be in two possible

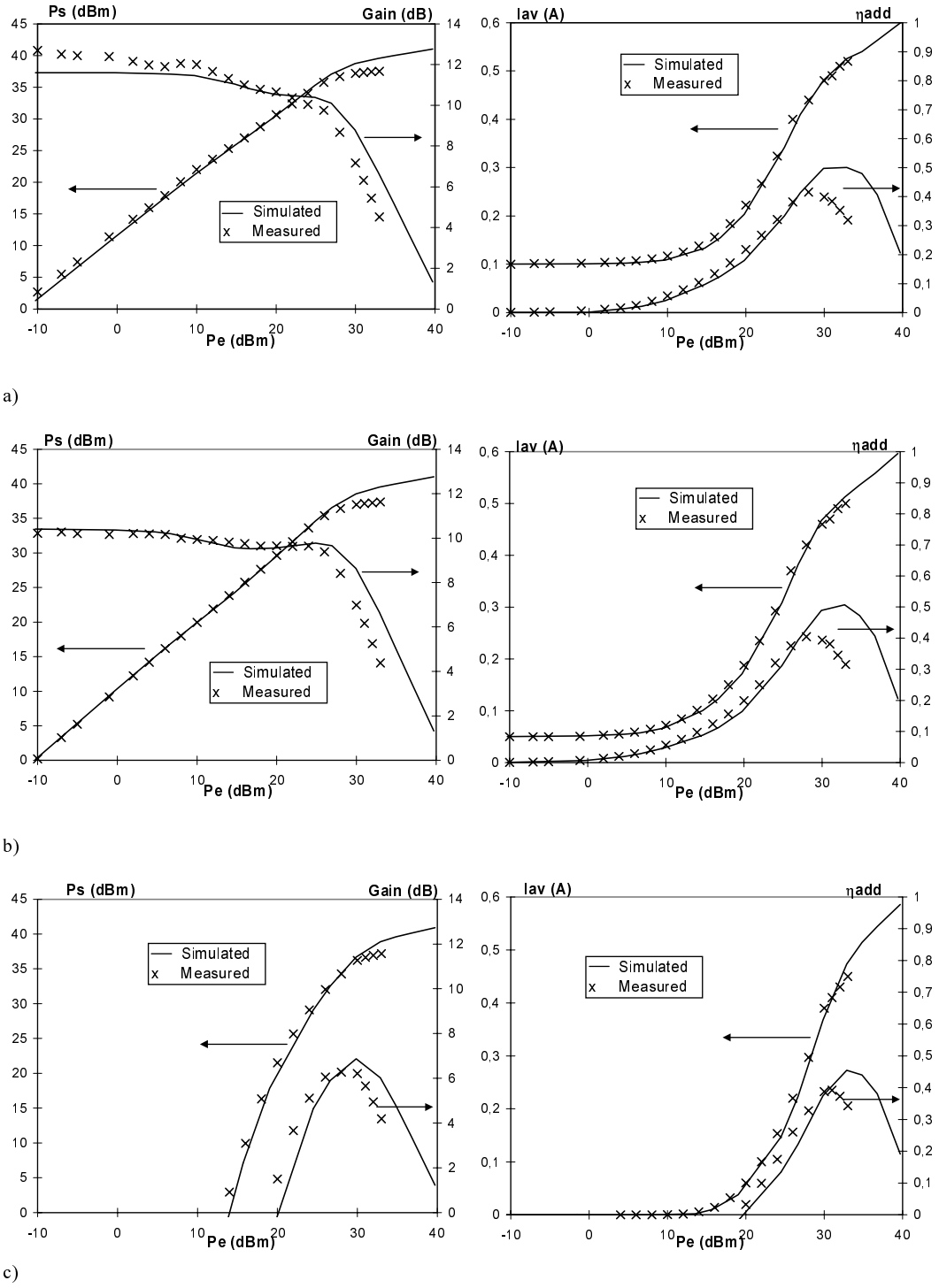

Fig. 14. Transfer characteristic $P_s(P_e)$, power gain $G(P_e)$, mean current $I_{av}(P_e)$ and power added efficiency $\eta_{add}(P_e)$: (a) $I_{DS0} = 100$ mA, (b) $I_{DS0} = 50$ mA, (c) $I_{DS0} = 0$ mA. $E_d = 26$ V, the working frequency is 2 GHz.

Table 2. Matching network impedance values in large signal mode.

Input network $Z_S = R_S + jX_S$		Output network $Z_L = \left(\frac{1}{R_L} + \frac{1}{jX_L}\right)^{-1}$	
R_S (Ω)	X_S (Ω)	R_L (Ω)	X_L (Ω)
2	5	70	30

configurations, series or parallel. The values determined for Z_S and Z_L (Tab. 2) are those which guarantee the maximum power transfer from the source generator to the transistor input and from the transistor output to the load, in the large signal mode at the 1 dB compression point, for a bias I_{DS0} of 50 mA. These impedance values are obtained by iterative method as it is described in the reference [14].

Figure 14 gives the comparison between measurements and simulations for the following characteristics:

(i) power transfer $P_s(P_e)$;
(ii) power gain G;
(iii) mean value of the drain current I_{av};
(iv) power added efficiency η_{add}, *i.e.* the ratio $P_s/(E_d I_{av} + P_e)$.

All these characteristics are given with respect to the radio frequency power P_e injected to the transistor input. The input power, the output power and the mean value of the current are calculated from a spectral analysis through a "Fast Fourier Transform, FFT" of the input signals I_g and V_{gs} and the output signals I_{ds} and V_{ds}, obtained in the steady state conditions.

The experimental characteristics present some properties:

- the mean current increases sharply at large signal level. When the compression rate becomes higher than 3 dB, the growth becomes linear with respect to the input power;
- the maximum output power and the mean current, when the component is operating under high compression rate, beyond 3 dB, are in the same order of value for whatever class of biasing;
- however, the gain is notably reduced when we change from class AB to class C. As a result, the maximum value of the power added efficiency is roughly the same for the two class. The highest value of about 42% is naturally obtained at $I_{DS0} = 50$ mA, the bias point at which the matching networks are tuned; this special situation impacts the class C results.

It can be noticed that the model accounts well of the experimental behaviour.

5 Conclusion

In this paper, we have established a new model, compatible with the circuit simulator PSPICE, for the LDMOS transistor used for power amplification in the frequencies band 1.8–2.2 GHz dedicated to the system DCS. More particularly, a new representation of the non-linear inter-electrode capacitances, gate-drain C_{gd} and drain-source C_{ds} was proposed. The proposed model was implemented in the simulator and validated for the radio frequency large signal amplification. A comparative study is carried out for the following characteristics:

(i) transfer $P_s(P_e)$;
(ii) power gain $G(P_e)$;
(iii) mean value of the drain current $I_{av}(P_e)$;
(iv) power added efficiency $\eta_{add}(P_e)$, at a working frequency of 2 GHz.

For all the studied cases, a good agreement is observed between the experimental and the simulation results. It appears that the proposed model can be used for the CAD of radio frequency power amplifiers.

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